Development and characterization of plasma etching processes for the dimensional control and LWR issues during High-k Metal gate stack patterning for 14FDSOI technologies

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Développement et caractérisation des procédés de gravure plasma impliqués dans la réalisation de grille métallique de transistor pour les technologies FDSOI 14nm : contrôle dimensionnel et rugosité de bord

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Development and characterization of plasma etching processes for the dimensional control and LWR issues during High-k Metal gate stack patterning for 14FDSOI technologies

(Abstract)

In a transistor manufacturing process, patterning is one of the hardest stages to control. Along with downscaling, the specifications for a transistor manufacturing have tightened up to the nanometer scale. Extreme metrology and process control are required and Critical Dimension Uniformity (CDU) and Line Width Roughness (LWR) have become two of the most important parameters to control.

So far, to meet the requirements of the latest CMOS technologies, post-lithography treatments such as plasma cure treatments have been introduced to increase photo-resist stability and to improve LWR prior to pattern transfer. However, conventional post-lithography treatments are no more efficient to address the specifications of 14nm gate patterning where more complicated designs are involved.

In this work, we have studied limitations of cure pretreatments in 2D gate integrations. In fact, the HBr plasma post-lithography treatment was identified as being responsible of a local pattern shifting that result in a loss of the device's electrical performance. Preliminary results show that, cure step removal helps to control pattern shifting but to the detriment of the LWR. Indeed, if no cure treatment is introduced in the gate patterning process flow, photoresist patterns undergo severe stress during the subsequent Si-ARC plasma etching in fluorocarbon based plasmas. In this work, the mechanisms that drive such resist degradation in fluorocarbon plasmas have been studied and improved SiARC etch process condition shave been proposed. Besides, we evaluate how the state-of-art gate etch process can be improved, by investigating the impact of each plasma etching step involved in the high-K metal gate patterning on both LWR and gate shifting. The goal of this study is to determine if the TiN metal gate roughness can be modified by changing the gate etch process conditions. Our research reveals that addition of N_2 flash steps prevents from gate profile degradation and sidewall roughening. In revenge, the TiN microstructure as well as the HKMG etch process has no impact on the gate final roughness. However, the TiN LER is strongly modified during the wet cleaning process. This modification results from the dissolution of TiN sidewall passivation layers that are formed during plasma processing. Although the TiN LER is also modified during wet process, the hard mask patterning process still remains the main contributor for gate roughening.

Keywords: Plasma etching, Gate shifting, Photoresist degradation, Roughness, HKMG, 14FDSOI.

Développement et caractérisation des procédés de gravure plasma impliqués dans la réalisation de grille métallique de transistor pour les technologies FDSOI 14nm : contrôle dimensionnel et rugosité de bord

(Abstract)

Dans le procédé d'élaboration d'un transistor, la définition des motifs de grilles est une des étapes les plus dures à contrôler. Avec la miniaturisation des dispositifs, les spécifications définies pour la structuration des transistors se sont resserrées jusqu'à l'échelle du nanomètre. Ainsi, le Contrôle Dimensionnel (CD) et la rugosité de bord des lignes (LWR) sont devenus les paramètres les plus importantes à contrôler. Précédemment, pour atteindre les objectifs définis pour les précédentes technologies CMOS, des traitements post-lithographiques tels que les traitements plasma à base d'HBr ont été introduits pour améliorer la résistance des résines aux plasmas de gravure et minimiser la rugosité des motifs de résine avant leur transfert dans l'empilement de grille. Cependant, ces méthodes conventionnelles ne sont plus satisfaisantes pour atteindre les spécifications des nœuds avancés 14FDSOI, qui font intervenir des schémas complexes d'intégration de motifs. Dans ces travaux, les limitations des traitements plasma HBr pour réaliser des motifs de grille bidimensionnels comme définis par les règles de dessin ont été mises en évidence. . En effet, il s'avère que les traitements par plasma HBr sont responsables d'un déplacement local du motif de grille, qui entraine sur le produit final une perte de rendement. Des résultats préliminaires montrent que le retrait de cette étape de traitement réduit le phénomène de décalage des grilles, au détriment de la rugosité des motifs de résines. En effet, les résines non traités par plasma subissent d'importantes contraintes lors de l'étape de gravure SiARC en plasma fluorocarbonnés, ce qui génère une nette augmentation de la rugosité de la résine qui se transfère par la suite dans les couches actives du dispositif. Dans cette thèse, j'ai étudié les mécanismes de dégradation des résines dans des plasmas fluorocarbonés. Cette compréhension a abouti au développement d'une nouvelle chimie de gravure plasma de la couche de SiARC qui limite la dégradation des résines. De plus, j'ai évalué comment le procédé complet de gravure de grille métallique peut être amélioré pour réduire la rugosité et la déformation des motifs en travaillant sur chacune des étapes impliquées. Le but de cette étude est d'identifier les étapes de gravure ayant un rôle dans la rugosité finale de la grille. Mes travaux montrent que l'ajout des étapes de nitruration limite la dégradation du profil de grille et de la rugosité des flancs. Au contraire, la microstructure du film de TiN ainsi que les procédés de gravure de grille métal n'ont pas d'impact sur la rugosité finale du dispositif. Cependant, nos travaux ont montré que les étapes de nettoyage ont un fort impact sur la rugosité finale du TiN dû à la dissolution des couches de passivation générées pendant les procédés de gravure par plasma. Mis appart cette modification de la rugosité du TiN lors des procédés de nettoyage, le transfert du motif de grille lors des étapes de gravure du masque dur reste toujours le principal contributeur de la rugosité finale de grille.

Mots Clés: Gravure par Plasma, déplacement de grille, Dégradation des résines, Rugosité, grille métallique, 14FDSOI.

Nomenclature

AFM Atomic Force Microscopy

ALD Atomic Layer Deposition

AR-XPS Angle Resolved X-ray Photoelectron Spectroscopy

CD Critical Dimension

CD-SEM Critical Dimension Scanning Electron Microscopy

CF Correlation Factor

CVD Chemical Vapor Deposition

DC Direct Current

ER Etch Rate

ESC Electro Static Chuck

FC Fluorocarbon

FDSOI Fully Depleted Silicon On Insulator

FTIR Fourier Transform Infra Red Spectroscopy

GS Gate Shifting

HK High K

HKMG High-K Metal Gate

HM Hard Mask

ICs Integrated Circuits

LER Line Edge Roughness

LSR Light Signal Reflectometry

LWR Line Width Roughness

Ne Electron Density

OES Optical Emission Spectroscopy

PR Photoresist

RF-PVD Radio Frequency Physical Vapor Deposition

RMS Root Mean Square

SiARC Silicon Anti Reflective Coating

SoC Spin on Carbon

STG Side Tuning Gas

Td Degradation Temperature

Te Electron Temperature

Tg Glass Transition Temperature

TGA Thermo Gravimetrical Analysis

VUV Vacuum Ultra Violet

XRD X-ray Diffraction

ACF Auto Correlation Function

ITRS International Technology Roadmap for Semiconductors

ME Main Etch

OE Over Etch

PSD Power Spectral Density

OPC Optical Proximity Correction

PAB Post Applied Bake

PEB Post Exposure Bake

PAG Photo Acid Generator

STI Shallow Trench Isolation

XPS X-Ray Photoelectron Spectroscopy

LELE Litho-Etch Litho-Etch

RIE Reactive Ion Etching

MOS Metal Oxide Semiconductor

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General Introduction

The microelectronic industry has been one of the most important industry sectors for the last 60 years. The first transistor was made by Bell laboratories in the late 40s. It was made up of a pure germanium crystal and its size was about the palm of a hand. From that day, the microelectronic industry has well developed. Today, transistors are nanometer scale devices made of a number of different materials stacked in complicated integrations. Now, transistors are the core of most of our electronic devices; from cars and mobile phones to pacemakers, and their applications are countless: Automotive, Biology, Security, Medicine...

Such a huge evolution is the result of a lot of hard work carried out by engineers and scientists whose goal was to improve the transistor manufacturing process in order to achieve the best performances. This led to a continuous decrease of the transistor dimension and an increase of the transistor density per chip. However, the pursuit for the transistor miniaturization results in an increased complexity of the integrated circuits and therefore, transistor manufacturing becomes more and more challenging.

To assist this increasing complexity, the "International Technology Roadmap for Semiconductor" (ITRS), defines every year the goals to be obtained by the semiconductor industry. Thus, in a transistor manufacturing process, gate patterning has become one of the hardest stages to control. Along with downscaling, the ITRS specifications for a transistor manufacturing have tightened up to the nanometer scale. Extreme metrology and process control are required and the gate Critical Dimension Uniformity (CDU) and Line Width Roughness (LWR) have become two of the most important parameters to control. In 2011, the ITRS affirmed that the gate CD non-uniformity should not exceed 10% (for 14nm technologies) while the LWR should not be higher than 12% of the gate dimension. In other words, for a gate pattern of 20nm, the ITRS predicts a gate size variation of 20±2nm with a sidewall roughness (LWR) of 2.4nm.

Nowadays, the best lithography conditions allow the definition of photo-resist patterns with a minimum roughness of 4-5nm and a CD non-uniformity of around 2%, which will be then transferred to the underlying layers by plasma etch processes. This means that in order to achieve the specifications defined for the latest CMOS technologies, new strategies need to be implemented to control this variability.
So far, post-lithography treatments such as plasma cure treatments have been introduced to increase photo-resist stability and to improve LWR prior to pattern transfer. However, conventional post-lithography treatments are no longer efficient to address the specifications for 14nm gate patterning where more complicated designs are seen.

The goal of this work is to evaluate the impact of subsequent etch steps in the dimensional control and LWR of a 14FDSOI gate pattern. Thus, the work is particularly dedicated to the understanding of the gate pattern deformations during the etch process and the LWR evolution at each process step.

The first chapter is dedicated to recall of the context in which this work has been carried out. A brief summary of the state-of-art is proposed followed by a discussion about the main challenges concerning gate patterning processes.

The second chapter is dedicated to the description of the experimental setup. In this chapter, a detailed description of the substrates and etch conditions is given. Besides, the operating principle of certain characterization techniques is described to better understand the results obtained in the following sections.

The third chapter describes the challenges encountered due to the addition of cure steps on 14FDSOI gate integrations where complicated 2D patterns are defined. A particular attention was paid to the understanding of the observed phenomena in order to propose solutions to prevent gate pattern degradation.

The fourth chapter, focuses more particularly on the photoresist degradation during the etch process. Besides, the evolution of the gate LWR during the hard-mask patterning process is studied.

Finally, the last chapter is dedicated to the study of the LWR evolution along a gate stack consisting in a polysilicon/metal/high-k stack. More particularly, the study is focused on the impact of High-K Metal Gate etch steps on the final gate roughness.

This was a CIFRE PhD carried out in collaboration with STMicroeletronics (ST) and the LTM Laboratory (CNRS). All the experiments were carried out in an industrial environment (i.e. Industrial reactor) and on real ST substrates to better answer to ST challenges in terms of CD control and LWR for advanced 14FDSOI technologies. At the beginning of this PhD, this product was in progress of development and was scheduled to be released by 2015.

Chapter I. Introduction

I.1 Microelectronic context

Microelectronics is the science that studies and manufactures integrated circuits at a microscopic scale. This includes the manufacturing of transistors, capacitors, inductors, diodes and a number of different electronic components.

The origin of the semiconductor industry stands in 1947, where the first bipolar transistor was developed over a germanium mono-crystal by J. Bardeen, W. Brattain and W.B. Shockley from Bell Laboratories [1]. However, it was only **in 1960 that this industry exploded thanks to the development of the first** transistor made of a metal deposed over an oxide and a semiconductor material, or **"Metal Oxide Semiconductor" (MOS) transistor**, by D. Khan and M. Attala [2].

Each MOS transistor allows the transfer of the electric charge, though the charge carriers could be either holes or electrons. Thus, two different transistors are defined: n-MOS transistors (when the transferred charges are electrons) and p-MOS (when the transferred charges are holes). To choose the charge carrier's nature, the substrates are doped either choosing N-type (i.e. Phosphor) or P-type dopants (i.e. Boron). A schematic representation of an n-MOS transistor operating principle is shown in Figure I.1.

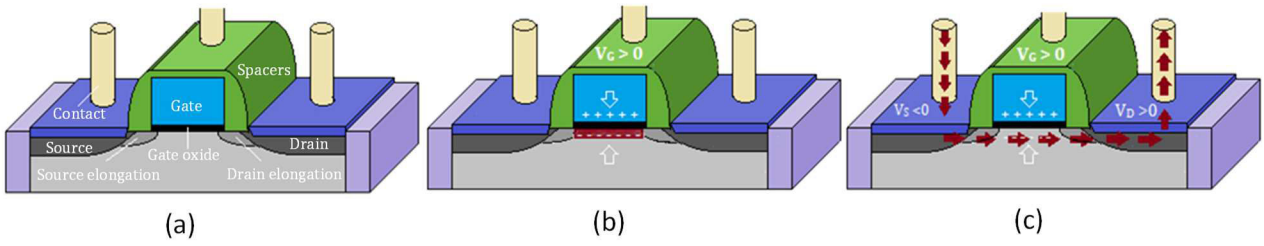


Figure I-1 Schematic representation of n-MOS transistor operating principle. (a) Illustration of the MOS components at V_G=0, (b) Formation of the conduction channel with a V_G>0 and (c) conduction of electrons at V_D>**0** [3]**.**

The n-MOS transistor is composed of four electrodes, the substrate (i.e. Silicon, P doped), the gate, the source (N doped) and the drain (N doped) (Figure I.1a). To each one of these electrodes, a different voltage will be applied, identified as V_G, V_S and V_D. When no potential is applied (V_G = 0), no charge is formed in the MOS junction. However, since the substrate potential is always kept to zero, if a potential is applied into the gate electrode (V_G> 0) an electric field is formed in the MOS junction. This electric

field will repulse the holes present in the semiconductor surface to create an N-type inversion channel where electrons will conduct (Illustrated by the red zone in Figure I.1b). Typically, the source potential is equal to zero (V_S=0) while the drain is elevated to a higher potential (V_D> 0). Therefore, the electron conduction occurs from source to drain (Figure I.1c).

The combination of n-type and p-type MOS transistors leads to a latter exploration of the CMOS technology (Complementary MOS), which allows the definition of the first logic functions and enabled the fabrication of integrated circuits. Thus, the first integrated circuit was then born in 1960, and the first microprocessor was built by Intel in 1971 [4]. Since then, **the dimensions of the integrated circuit main elements (i.e. the MOS transistors) have been progressively reduced to improve their performance and reduce the manufacturing costs.** This led to an explosion of the semiconductor market in order to offer smaller products to the consumers that integrate more functionalities. Thus, in 1974, the Moore's law was established, an economic trend that forecasted that the number of transistors composing a microprocessor should double every two years [5]. This trend was followed by the formation of the ITRS (International Technology Roadmap for Semiconductor) in 1997, an industrial organization that predicts the evolution of the microelectronic industry and defines the goals to be achieved for the years to come. As an example, the gate dimensions defined by the ITRS in2011 for the following years are listed in Table I.1 [6].

Table I-1 Gate length evolution between 2012 and 2017 as defined by the ITRS 2011

Year of Production	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**
Gate length (nm)	22	20	18	17	15	14	13	12	11

Therefore, the semiconductor industry has increased the complexity of the developed transistors in order to achieve the ambitious goals defined by the Moore's law and the ITRS. This increased complexity includes reduction of gate dimensions, addition of new materials into gate stacks, improvement of the masking strategies and the development of new manufacturing processes. Figure I.2 illustrates the gate length evolution as predicted by the 2011 ITRS compared with the gate length as defined by the Moore's law.

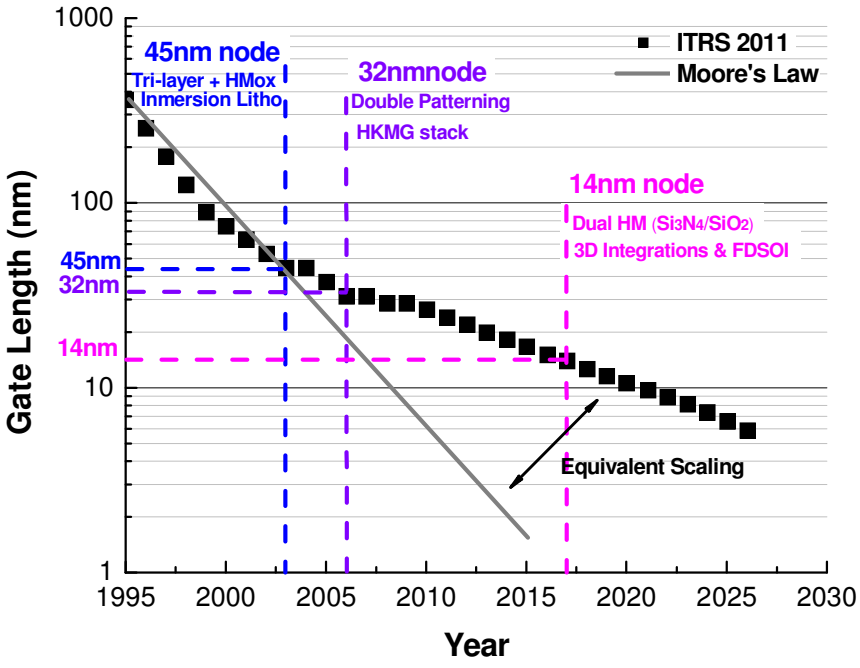


Figure I-2 2011 ITRS predictions for the gate physical length evolution between 1995 and 2030. The ITRS trend is compared to the gate length evolution as defined by the Moore's law. After the 45nm node, the difficulties to obtain performing MOS transistors lead to a change in the gate integrations. Reprinted from ITRS 2011 [6].

As it can be observed in Figure I.2, the first gate integrations (i.e. before 45nm technologies), agree with the trends defined by the Moore's law. At that time, the transistors were carried out with the classical MOS stack, which consisted in a polysilicon gate over a silicon gate oxide layer. However, along with transistor downscaling, more aggressive targets were defined in terms of gate dimensions and uniformity control. This resulted in an increased complexity of the transistor manufacturing process, and more particularly reviewing the masking strategies, and materials stacks used for feature definition.

As an example, Figure I.3 shows the gate stack evolution from the 120nm node until the 14nm node. In the first raw, the full gate stack is schematically illustrated where the increasing stack complexity, and the reduced dimensions are also described. In the second raw, TEM images of the gate stacks after full etch are also shown.

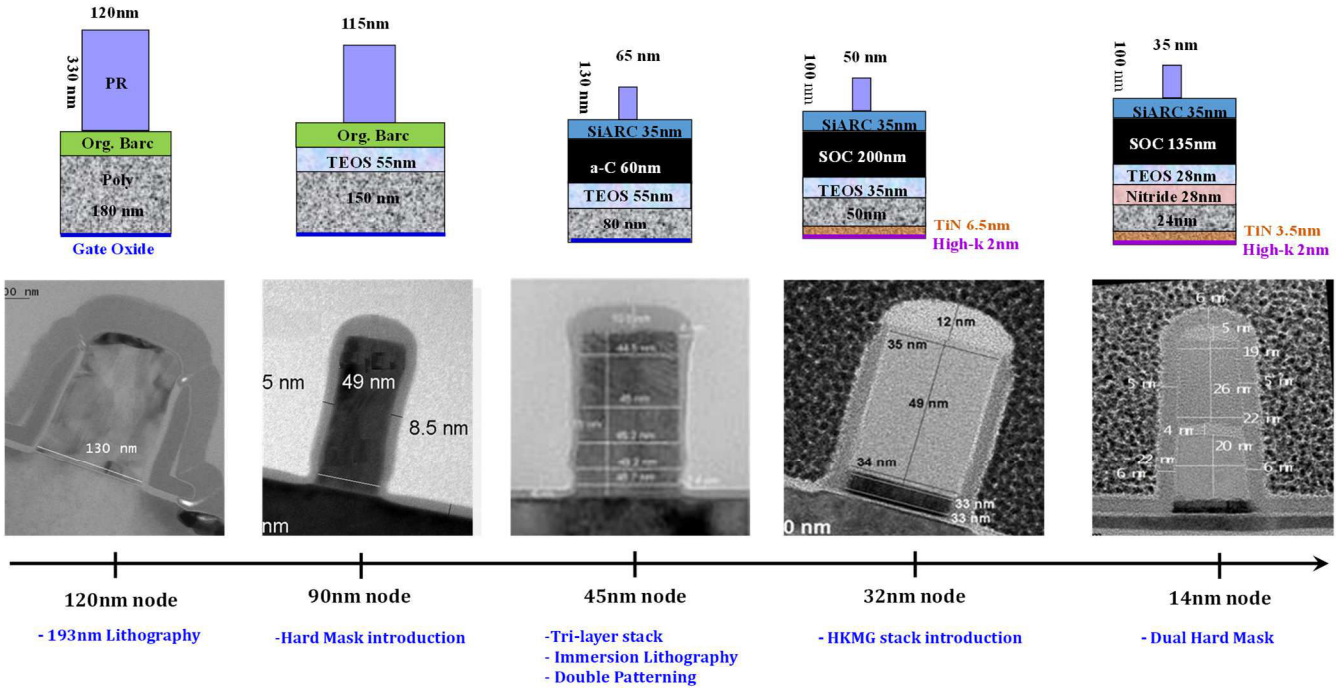


Figure I-3 Gate stack evolution from 90nm to 14nm technological nodes

Initially for the 120nm node, the gate patterns were defined using a simple photoresist mask (Fig I.3); and the gate dimensions were reduced by only reducing the photoresist pattern dimensions. However, due to the limited photoresist budget, this strategy was not adapted to define smaller gate patterns. Thus, already for the 90nm node, oxide hard masks were introduced (Fig I.3). With this strategy, the pattern dimensions were still reduced by reducing the resist pattern dimensions, while the hard-mask was used to improve the pattern transfer into silicon. However, below the 45nm node, the classic lithography could not resolve the novel design targets and other strategies, such as, tri-layer lithography stack depositions, immersion lithography and double patterning techniques had to be implemented to achieve the gate patterning (Fig I.3) (i.e. these new strategies will be further described in section I.3).

However, the smaller the gate dimensions, the more challenging becomes the MOS manufacturing and as it can be observed in Figure I.2, for the 32nm node and beyond, the gate length predicted by the Moore's law cannot be reached, and we slightly move away from the specified trend. This deviation occurred because the small MOS devices undergo a loss in their electrical performances due to physical failure effects such as, polysilicon depletion [7] or gate leakage because of the extreme reduction of the oxide thickness [8]. As a result, the engineers realized that it was not possible to continue with the classical CMOS downscaling and other strategies need to be found. Thus, with the arrival of the 32nm node, TiN metal and HfSiON high-k materials were added into the gate stack leading to the first HKMG integrations (Fig I.3). This marked a breakdown for the semiconductor industry, which moved into a new trend, based in an "*Equivalent Scaling*", which consists in carrying out bigger transistors but with optimized gate integrations that allow reaching performances that are equivalent to those of "ideally" small transistors (Fig I.2).

Taking advantage of this new scaling trend, the transistor downscaling continued its course until the 14nm node. For this new integration the gate stack was again in order to meet the specifications. In fact, due to the continuous reduction of the oxide layer thickness, the HfSiON high-k material was no longer efficient to avoid gate leakage and was replaced by HfO_2 materials [8]. Besides, due to manufacturing modifications, the traditional oxide hard mask was not sufficient to assure suitable gate patterning and

the masking strategy was also improved by addition of a dual hard masks formed by SiO_2/Si_3N_4 stacks (Fig I.3).

However, to keep on with the ITRS downscaling, modifying the gate stacks seemed not sufficient. The gate leakage effects due to the extremely thin oxide layer depositions and the limited control of source and drain electrodes become important failure sources, and new transistor integrations are required. Some industries such as IBM and Intel bet for 3D integrations like FinFET integrations. Such transistors are based on fins on which field effect transistors are built and are wrapped around by the gate structures (Figure I.4a). These 3D structures are assumed to achieve higher performances at lower voltages; however, they suppose an increase challenge in terms of manufacturing [9] [10].

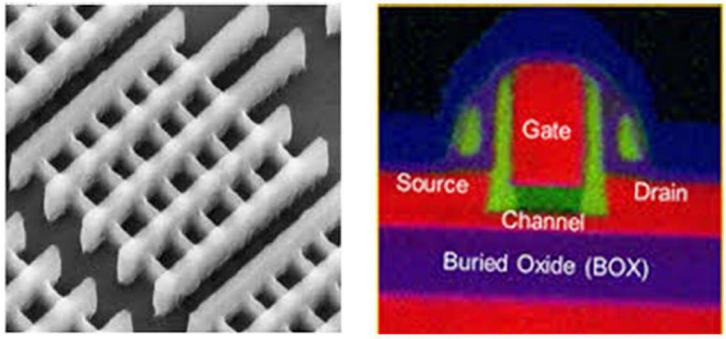


Figure I-4 SEM image of a FinFET and (a) TEM-EDX image of a FD-SOI gate integration. In (b) different materials are identified by different colors.

Other companies, like STMicroelectronics, preferred remaining on planar structures, and bet for new strategies such as the « Fully Depleted Silicon On Insulator" (FDSOI) integrations (Figure I.4b). The idea is to add a buried oxide (BOX) within the silicon substrate to physically limit vertically the source and drain zones and reduce the leak currents between the junctions and the substrate. This enables a better control of the gate electrode (V_G) on the carrier density conduction along the conduction channel [11]. This strategy should help to achieve the performances established by the ITRS without moving into more complicated 3D integrations.

This PhD work was carried out at STMicroelectronics, and is therefore focused on the development of the 14FDSOI technologies with 14nm gate integrations, or in other words, HKMG integrations on SOI wafers.

I.2 Electronic circuit manufacturing

The 14FDSOIintegrated circuit manufacturing process counts with more than 300 technological steps and is divided into five main sections (Figure I.5).

1. **Active zone and Isolation trench (STI) formation:** To separate N-MOS and P-MOS active zones present within the SOI substrate.
2. **The Gate fabrication:** The formation of the transistor MOS junctions.
3. **Formation of the gate spacer and Source & Drain areas**: Dopant implantation to form the Source and drain regions. Spacers are deposited to avoid short-cuts between source, drain and gate electrodes.
4. **Contact Formation**: Deposition of the first metal layer (in W) over each electrode (Gate, Source & Drain) to enable interconnection.

5. **Interconnection**: elaboration of the 9 different metal levels (in Cu) that allow the connection between different transistors.

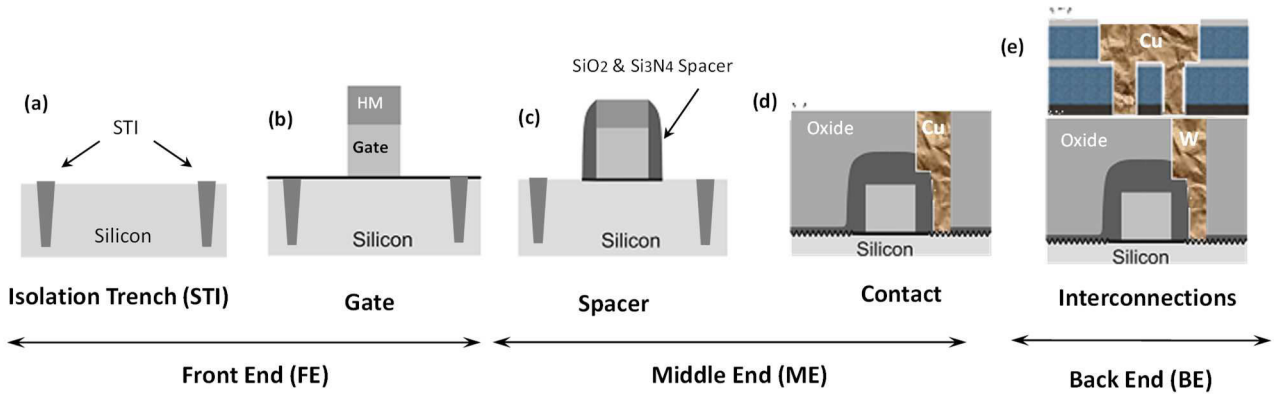


Figure I-5 Five main sections involved in the 14FDSOI integrated circuit manufacturing: (a) STI formation, (b) Gate formation (c) Spacer deposition and implantation of source and drain electrodes, (d) Contact of all Source, drain and gate electrodes by a first W metal layer (To simplify, only the drain contact is shown) and (e) Interconnection of all the transistors by the formation of 9 different metal levels using Copper (Cu) as connection metal.

These five sections are grouped into three main stages: The "Front End of line" (FE) which involves the fabrication of the active part of the integrated circuit (the transistors) (cf fig I.5 a, b); the "Middle End of line" (ME) for the fabrication of the first contact levels (cf. fig I.5c, d), and the "Back End of line" (BE) (cf.fig I.5e) which includes the fabrication of the different metal interconnections that allow the communication between different transistors.

To develop each one of these structures (Active, Gate, Spacer…), typically a four step process flow is followed:

1. Material deposition and polishing (to flatten the material surface).
2. Lithography, to imprint a pattern into a photoresist
3. Etch, which transfers the photoresist pattern into the whole material stack by plasma or wet processes
4. Wet cleaning, to remove the residual polymers after etch processes.

Some of the described sections can also include other process steps such as: Epitaxial crystalline material growth (i.e. for Contact fabrication), implantation (i.e. the introduction of particular chemical elements into materials for example for the formation of Source & Drain zones) and thermal treatments.

In my PhD, I have worked on the FE process, and more particularly on the development of plasma etch processes for 14nm gate patterning.

I.3 Gate Patterning

Gate patterning is carried out following a top-down approach. This consists in using two different steps for material structuration: The lithography, where the gate pattern is imprinted over a photoresist film, and the etching process, where the photoresist pattern is transferred into the remaining gate stack.

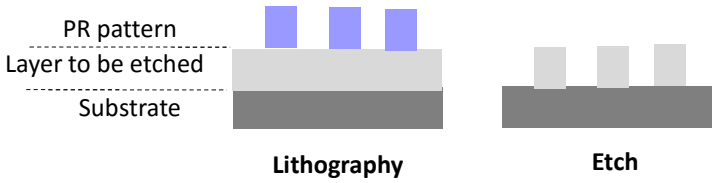


Figure I-6 Schematic representation of the top-down approach

I.3.1 Lithography

The lithography consists in the definition of gate designs into a photoresist film and is therefore the stage where the dimensions of the imprinted features are defined. Thanks to the improvements done at this manufacturing level, the pattern's Critical Dimension (CD) is reduced and the transistor density within a wafer can be increased.

A schematic design of the complete lithography process is shown in Figure I.7.

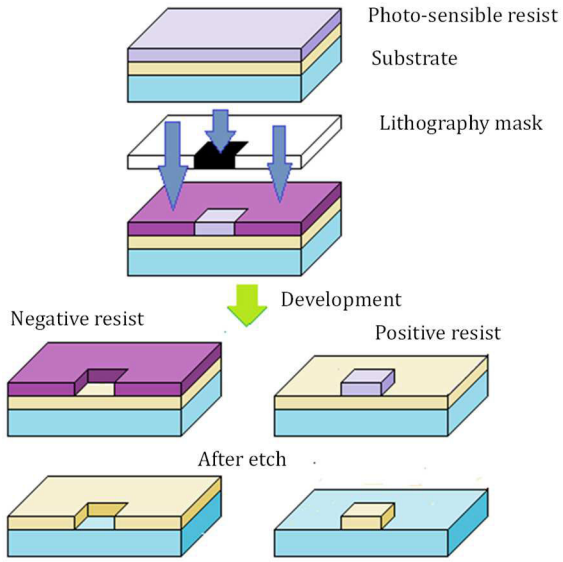


Figure I-7 Principle of lithography [3]

In the lithography process, the photoresist film is exposed to UV irradiation through a quartz mask where the desired gate features have been designed. This mask covers certain parts of the photoresist while the remaining film is exposed to the UV irradiation. Under exposure, the resist undergoes several chemical reactions that make it soluble in a specific solvent (i.e. Developer, typically TMAH for "Tetra-Methyl Ammonium hydroxide"). The difference in the solubility between the exposed and un-exposed resist allows imprinting the mask features into the photoresist film (i.e. for positive zone PR). This process is carried out in five steps:

1. **Layer deposition:** First, the lithography tri-layer stack is deposited over the polysilicon wafer using the Spin Coating technique. This consists in: an amorphous carbon planarizing layer (Spin on Carbon SoC), that improves the surface uniformity of the polysilicon wafer; an anti-reflective coating (SiARC), which absorbs the reflected wavelengths and avoids photoresist pattern degradation by UV back scattering; and the photoresist (PR) which consist in a chemically amplified resist.

Chemically amplified photoresist are extremely sensitive resist materials that by action of one only photon undergo several chemical reactions. These photoresist include: a *polymer* (composed of different monomers that improve the PR thermal stability, adhesion or etch resistance…), a *Photo-Acid Generator* (PAG, containing photo-catalytic groups which under UV exposure are transformed into acids), and a *quencher* (i.e. a basic component that limits the photo-catalytic reaction and controls the acid diffusion within the photoresist film).

2. **Post applied bake (PAB):** Is a soft bake condition (T~100ºC) used for solvent desorption and resist densification after deposition. The PAB temperature is chosen so that no thermal degradation of the un-exposed photoresist occurs during the baking process and is therefore dependent on the polymer material.

3. **Exposure:** consist in the exposition of the photo resist to a specific wavelength through a lithography mask. Due to this exposure, the PAG undergoes photo-catalytic reactions that lead to acid formation. An example of the photo-catalytic reactions using a "tri-phenyl-sulfonium antimony hexafluoride" PAG is shown in figure I.8 [12].

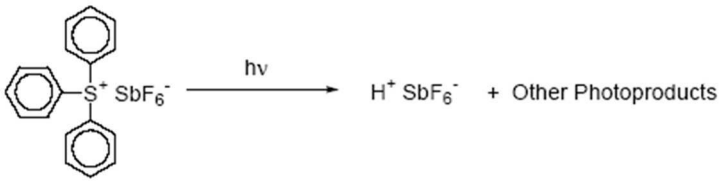


Figure I-8 Tri-phenyl-sulfonium antimony hexafluoride Photo Acid Generator (PAG) photo-catalytic reaction to form $H^+SbF_6^-$ acids. [12]

4. **Post Exposure Bake (PEB):** In this step, the photoresist is heated until the activation temperature for the photoresist deprotection reaction is reached. At this temperature, the acids (H^+) generated by the PAG photo-catalytic reaction react with the polymer material which undergoes an ester photolysis. This results in the cleavage of each monomer's active groups and the formation of soluble resist material. The PEB temperature is dependent on the activation energy for the deprotection reaction, and therefore changes from one polymer to another. A schematic representation of the polymer deprotection reaction is shown in Figure I.9 [13].

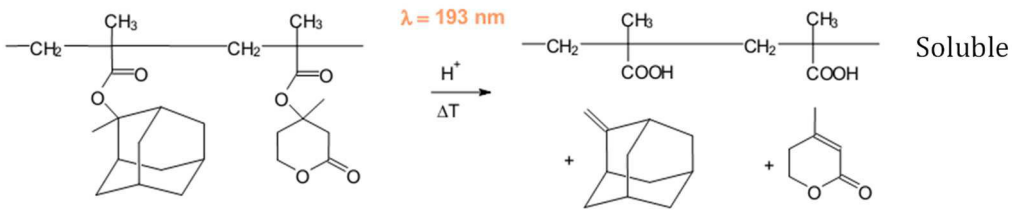


Figure I-9 Example of the deprotection reaction of a AZ/Clariant193nm Photoresist in presence of an acid (H+). Ester hydrolysis leads to a detachment of monomers active groups and the formation of a soluble polymer backbone in basic solution [13].

5. **Development:** In this final step, the exposed polymer material is dissolved selectively towards the non-exposed material using an adapted solution. In the given example, since the resulting polymer matrix presents an acid nature, it will be soluble in basic solutions such as TMAH. This results in the transfer of the mask features into the photoresist film.

I.3.2 Etch

Once the photoresist patterns have been defined by the lithography step, the etching processes will be used to remove the material from the zones that were not covered by the photoresist (c.f Figure I.7).

Depending on the applications, the photoresist pattern transfer can be carried out using either the wet etching or the plasma etching.

Historically, wet etching was used for pattern transfer. This technique is very **selective** and allows the removal of a material's layer without damaging the underlying materials. In the latest technologies, for example for the 28nm node, it is still used for the elaboration of N-MOS and P-MOS HKMG integrations [14]. However, wet solutions lead to an **isotropic** etching of active materials where the directionality of the etching process cannot be controlled. Along with downscaling, wet etching became less suitable for the definition of small patterns and an increasing interest grew towards plasma etching processes.

Plasma etch processes are **less selective** than wet processes but **anisotropic,** and allow transferring the lithography patterns vertically into the whole gate stack. Thanks to the definition of vertical gate patterns, a strong fidelity and an improved dimensional control can be obtained.

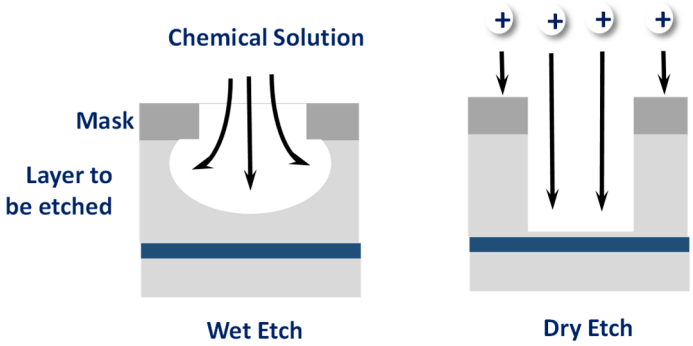


Figure I-10 Differences between a wet etch process and a plasma etching process [15]

For the gate patterning process, since complicated gate stacks with a number of different materials need to be etched with an extreme pattern fidelity and anisotropy, plasma etch processes are preferred.

I.3.2.1 Plasmas used for dry etch processes

A plasma is an ionized gas that is composed of ions(positive and negative), electrons, and neutral species (molecules, atoms and radicals). These species interact between each other and result in a globally neutral environment.

Each plasma is characterized by its **electron density**, n_e (i.e. the amount of generated plasma electrons) and the **electron temperature**, T_e (or the average kinetic energy of plasma electrons). Thus, depending on these two magnitudes different types of plasmas can be described such as "hot plasmas" (i.e. T>10^6K,

which are typically used in fusion physics) and "cold plasmas" ($T<10^6$K, typically used for microelectronic applications).

For Microelectronic applications, we will therefore use "Cold plasmas" at low pressures (i.e. 1mT-1T). These are plasmas in a non-thermodynamic equilibrium (i.e. the electron temperature (T_e~2-3eV) is very superior to the ion temperature (T_i<0.1eV)) where the ion (and electron) proportion (~10^8–10^{12} cm^{-3}) is low as compared to the proportion of neutral species (~10^{13}-$10^{17}$$cm^{-3}$).

For our applications, plasmas are generated in an "inductively coupled plasma" (ICP) reactor where the gas is confined between two electrodes. When a certain voltage is applied, an electric field builds up and the electrons absorb enough electrical power to be heated. These energetic electrons collide with the surrounding neutrals and sustain the plasma discharge by the formation of plasma species. As a result of these collisions, several chemical reactions may occur:

Dissociation: $e^- + A_2 \rightarrow 2A + e^-$

Ionization: $e^- + A \rightarrow A^+ + 2e^-$

Excitation: $e^- + A \rightarrow A^* + e^-$

Generally, the excitation reactions are always followed by a relaxation reaction ($A^* + e^- \rightarrow A + h\upsilon$) that leads to the formation of energetic photons (VUV) that contribute to the etch process (i.e. photoresist modification, default generation, photo-etching…) [16] [17]

An important notion on the plasma discharge is the frequency at which electron/neutral collisions occurs. Thus, the electron **mean free path (λ)**, represents the average distance that an electron can cross without colliding with another molecule within the gas phase. This distance depends on the electron temperature and the gas pressure and is described by the following formula:

$$\lambda = \frac{kT}{\sqrt{2}\pi d^2 P} \qquad \text{(Eq. I.1)}$$

Where, k is the Boltzmann constant (1.38x10^{-23} J/K), T is the gas temperature in K, d is the particle diameter in meters and P is the gas pressure in Pascal.

Depending on the mean free path, electrons will undergo more or less collisions within the gas phase where they will lose a certain part of their energy. Thus, the **ionization degree** (**α**) of a plasma, or the ratio between ion density and the neutral density, depends on the amount of collisions happening within the gas phase that is dependent on the electron density and temperature (ne and Te). For microelectronics, the plasma ionization degree is typically less than 10^{-2}. At the same time, the electron density (n_e), typically of 1x10^{11} cm^{-3}, is directly related to the applied electrode power, while the electron temperature (T_e), typically of 2-3eV, is dependent on the working pressure.

I.3.2.2 Plasma etch mechanisms

The main interest on plasma etching or Reactive Ion Etching (RIE) is the possibility to combine chemical etching (to improve the selectivity) and physical etching (to increase anisotropy).

a) Chemical etching

Chemical etching involves the reactions taking place between reactive radicals and material surfaces. For example, if we consider silicon etching in SF_6 plasmas, the chemical etching mechanism consists in four mains steps described as follows [18] [19] [20]:

1. Creation of reactive radicals in gas phase
   i.e. $SF_6 + e^- \rightarrow SF_5 + F + e^-$
2. Adsorption of reactive species on the silicon surface
   i.e. $Si + F \rightarrow SiF$
3. Formation of volatile reaction products
   i.e. $4F + Si \rightarrow SiF_4\,(g)$
4. Desorption of reaction products

This reaction is also possible with other halogens such as Chlorine and Bromine leading to the formation of $SiCl_4$ and $SiBr_4$ volatile species. Since the etching mechanism is based on a thermodynamic reaction, the chemistry choice is done depending on the material to be etched, so that the reaction products are stable volatile compounds. For example, silicon oxide is typically etched in fluorocarbon based chemistries by the formation of SiF_2, SiF_4, CO and CO_2 volatile compounds [21]. Carbon based photoresist are etched in oxygen based plasmas and several metals such as Aluminum are only etched in chlorine based chemistries [22].

Thus, the chemical etching is an isotropic process that is responsible for the improved selectivity during a plasma etching process. In fact, a specific chemistry can be chosen whose radicals are reactive to one of the materials, and form volatile compounds, while they are not reactive towards a second material. Thus, really good selectivities can be obtained for thin film etching in a presence of a patterned mask.

b) Physical etching

Physical etching corresponds to a material sputtering when it is exposed to an energetic ion bombardment. When an ion collides with a material, the material's surface atoms receive enough energy to be removed from the material surface.

This process is defined by the **etch yield (Y)**, or, the number of surface atoms removed per incident ion; and is theoretically represented as follows [23] [24]:

$$Y = A \times \sqrt{E_i - E_{th}} \qquad \text{(Eq.I.2)}$$

Where, A is a proportionality factor that is dependent on the incident ion sputtering angle, E_i is the ion energy and E_{th} is the threshold ion energy, or the minimum energy required for surface sputtering, which is dependent on the target material nature, and the incident ion nature. Therefore, the sputtering of a surface atom only occurs if $E_i > E_{th}$.

For lower ion energies (E_i ~0-10eV), other reactions may also occur at the substrate surface, such as, the migration of adsorbed species (i.e. Fluorine), the reorganization and mixing of the reactive surface layer and desorption of surface species.

Thanks to the directionality of incident ions during a physical sputtering process, a good anisotropy can be obtained, but, the etch selectivity is reduced.

c) Radical/ion Synergy

In a plasma etching process the advantages of chemical etching and physical etching are combined. Therefore, a good selectivity can be obtained, thanks to the selective reactions of radical species and also a good anisotropy is obtained, due to the directional ion bombardment.

Besides, the etch rates are strongly increased compared to the etch rates obtained for chemical or physical etching processes separately. This is due to the combined effect of radicals and ions. Ion bombardment enhances atom bindings breaking in the substrate surface. This leads to an increased adsorption of radicals and helps the formation of volatile species. Desorption of such species is also improved by the ion bombardment which generally speeds up the etching process [25]. Thanks to this radical/ion synergy the plasma etch processes are great interest for pattern transfer.

The plasma etch mechanisms are based in the fact that radical species and ions do not have the same angular distribution. The neutral species are isotropic, and lead to a lateral etching; while the ions, are anisotropic and are accelerated towards the substrate (i.e. by the electrostatic sheath). This results in a directional etching that speeds up the vertical etch rate as compared to the lateral etch rate and therefore a good anisotropy can be obtained.

To further decrease the lateral etching component and improve the anisotropy, passivating agents can be introduced in the gas phase. These are molecules that present a high sticking coefficient that are deposited on all the surfaces exposed to the plasma. These molecules can be adsorbed in the pattern sidewalls during the etching process to form a thin passivation layer that block the lateral etching. Therefore, the lateral etching on pattern sidewalls results from a deposition/etch competition that is driven by two components: the lateral etching induced by reactive radicals and the sidewall deposition promoted by sticky molecules.

To better explain the principle of the reactive ion etching (RIE) processes, Image I.11 illustrates the mechanisms taking place during a simple patterning process.

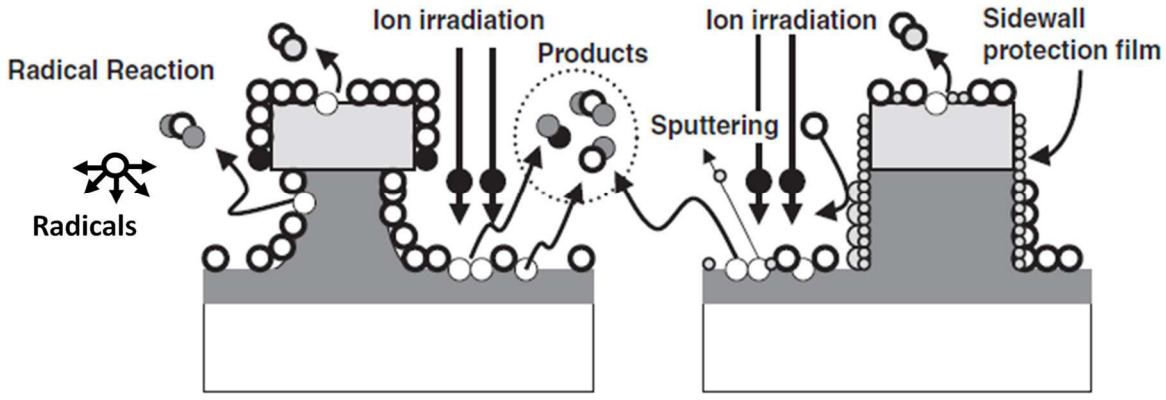


Figure I-11 Schematic representation of the mechanisms happening during plasma etching [79]

The passivating molecules can be either added intentionally to the gas phase (i.e. CH_2F_2 addition) or are produced during the process due to the formation of non-volatile etch by-products (i.e. $SiBr_x$ species) Depending on the plasma process conditions, the main two passivation mechanisms are:

- **Sidewall passivation formed from gas phase:** As an example, we can consider the silicon etching process in HBr/O_2 chemistries [26]. In this process, the Silicon is etched in HBr chemistries by formation of $SiBr_4$ volatile species. In addition less volatile $SiBr_x$ bi-products can be released into the gas phase and redeposit on all the surfaces exposed to the plasma and more specifically on the pattern sidewalls. There, they can be oxidized by oxygen radicals present in the plasma phase and form a thick SiO_xBr_y passivation layer that protects the profile from lateral etching. The passivation layers obtained by this mechanism present a non-uniformity of the passivation thickness along the sidewall and are typically thicker at the top of the etched patterns. (cf. Figure I.12a)
- **Sidewall passivation formed by by-product sputtering from the bottom of the structures:** Also known as *"Direct line of sight deposition mechanism"* [27] [28]. It has been shown that the silicon etch of horizontal surfaces proceeds through the formation of a fluorocarboned layer [29]. This fluorocarbon deposition is then sputtered from the bottom of the pattern due to ion bombardment and is re-deposited over silicon sidewalls forming a uniform passivation layer over the whole gate profile (cf. Figure I.12b).

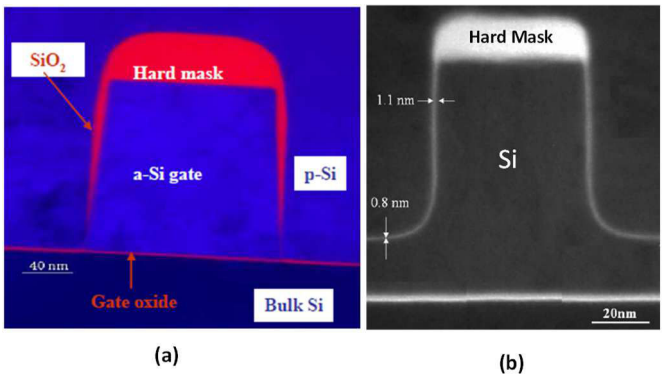


Figure I-12 TEM images of silicon gate patterns etched in (a) HBr/O_2 and (b) SF_6/CH_2F_2 plasmas.

The development of plasma etch processes is based on a fine comprehension of the passivation layer formation mechanisms which are key parameters to obtain anisotropic etch profiles.

d) Profile deformation mechanisms during plasma etching

As explained in the previous section, the plasma etch processes are ruled by the flux of neutral species (etching or passivating species) and the ion flux bombarding the surface. Depending on these two components, the patterning processes can undergo different modifications that degrade the patterned profiles. Depending on the origin of these deformations, we can differentiate three different mechanisms for pattern degradation:

Due to the difference in the ratios of neutral species and ions, there is a competition on the passivation/etch mechanisms that induce pattern deformations such as, undercutting and formation of tapered profiles.

- **Undercut**: consists in a lateral etching of the pattern sidewalls often due to a lack of passivation. For example, silicon etching in SF_6 plasmas without addition of any passivating agent may lead to silicon undercut (Fig I.13a).

- **Tapered profiles**: If the Passivation/etch mechanisms are not well controlled, the mask's dimensions may be modified which leads to the formation of tapered profiles. For example, if the sidewall deposition over the mask is too strong, the mask width can be progressively increased during the etching process leading to tapered profiles [30](Figure I.13b). The same may occur when the mask is consumed due to ion bombardment [31]. If we consider for example a PR mask, the sputtering yield is more efficient at 60º and therefore, the mask's sharp corner are eroded [32]. If the mask is eroded significantly, then, the bottom edge will also move leading to a tapered profile [33].

Other profile deformations, such as bowing, notching and micro-trenching, are caused when ions are directed towards the substrate with an off-normal incident angle. This is most likely due to charging effect [34], but can also be influenced by ion's transversal temperature [35] or ion scattering on hard mask facets [36]. These three phenomena are illustrated in Figure I.13.

- **Bowing**: is a CD loss under the mask level because the ion trajectory is distorted and they are directed towards the sidewalls (Fig I.13c). This effect is typically observed in the etching of low-k materials because they are fragile and they are etched following an ion enhanced etching mechanism [37].

- **Micro-trenching:** Though most incident ions are perpendicular to the substrate surface, they also present a lateral component that affects their trajectory. In some cases, they can also be reflected and displaced along the pattern vertical sidewall leading to higher ion fluxes near the base of the feature. This effect is called micro-trenching [38] (Fig I.13d).

- **Notching**: The notching effect is the lateral etching of underlying layers during the etch process (Figure I.13e). This can occur either due to positive charging of the underlying layer, which can deflect the ions towards the sidewalls (i.e. at low bias voltages) [39], or due to isotropic etching of sidewall passivation layers [40].

And finally we find the deformations related to the etch rate uniformity and the CD control such as loading and Aspect Ratio Dependent Etching (ARDE) effects.

- **Loading**: Consists in a consumption of the reactive species by the wafer or the reactor walls that results in a reduced etch rate. In practice, it results in a decrease of the etching rate with an increase in the amount of exposed material to be etched. The loading effect can be observed at a wafer scale (macro-loading) or locally at a feature-scale (micro-loading). The loading effect depends on the density of the features to be etched, the chamber volume (i.e. larger volumes reduce the loading effect) [32], the gas flow rate (i.e. ER increases with increasing flow rate) [41]and the lifetime of the reactive species (Fig I.13 f).

- **Aspect Ratio Dependent Etch rate (ARDE)**: is the etch rate dependence on the aspect ratio of the structure to be etched. This effect is attributed to the difference in flux of neutral species, ions, and ion energy as a function of the pattern aspect ratio and results in a lower ER for structures having higher aspect ratios. This issue is mostly important for hole or trench etch processes (Fig I.13 g).

A schematic representation of all the etch degradation mechanisms is shown in Fig I.13.

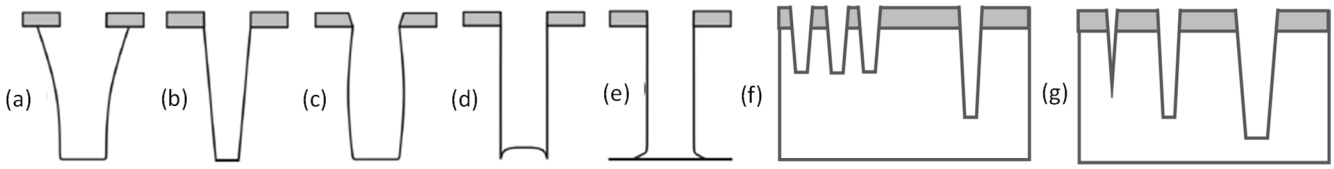


Figure I-13 Schematic representation of the gate profiles obtained during plasma etching: (a) Undercut (b) tapered profile (c) bowing (d) micro-trenching (e) notching, (f) Micro-loading and (g) ARDE.

All these profile degradation mechanisms become even more critical for gate integrations where small gate patterns need to be etched with strong uniformity and pattern fidelity.

I.4 Challenges in Gate Patterning

As already explained, for the gate patterning process, lithography and etch steps follow each other to carry out the definition of gate patterns. However, with the increased complexity of the gate stacks and the dimension reduction, the gate patterning process becomes more and more challenging. Therefore, in this section, we will discuss about the main challenges encountered for both, lithography and plasma etching processes that limit the definition of ultimate gate patterns.

I.4.1 Challenges related to the lithography step

To ensure a good photoresist pattern definition, lithography has to meet three requirements: Resolution, Sensibility and Roughness.

I.4.1.1 Resolution

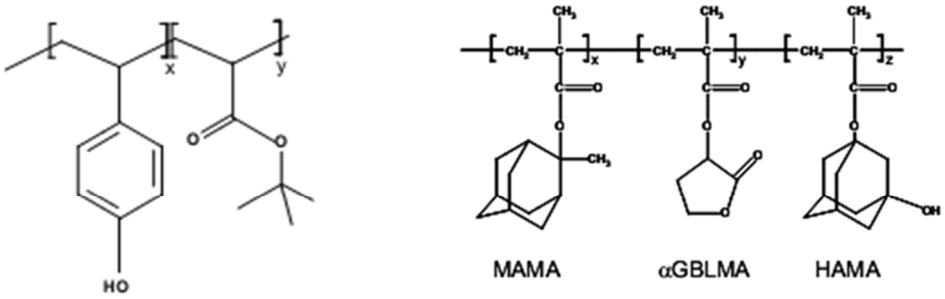
The Resolution (R) is the smallest interval feasible between two photoresist patterns. Along with downscaling, the lithography needs to achieve the definition of smaller photoresist patterns and for this, the image resolution at very small scales needs to be improved.

The lithography Resolution (R) is expressed by the following Rayleigh criteria:

$$R = k\frac{\lambda}{NA} \qquad \text{(Eq. I.3)}$$

Where k is an empirical constant (varies between 0.5-1 and depends on process conditions), λ is the light wavelength used for the PR exposition and NA is the numerical aperture of the lithography system (proportional to the environment refraction index, n, and the size of the optical lenses).

To improve the pattern resolution, it seems clear that the exposition wavelength (λ) needs to be decreased. This is the reason for which at the late 90s we moved from KrF lasers emitting 248nm light towards ArF lasers with a 193nm light emission. Clearly changing the exposition wavelength also implies adapting the photoresist materials. Thus, the photo-resist platforms evolved from 248nm based photoresist towards 193nm photoresists. An illustration of both resist platforms is shown in Fig I.14.



(a) 248nm Photoresist (b) 193nm Photoresist

Figure I-14 Structure of a (a) 248nm photo-resist based in a poly(hydroxystyrene) polymer matrix and a (b) 193nm photo-resist composed of three monomers: Methyl adamantane (MAMA) for thermal stability, a lactone group (αGBLMA) to improve PR solubility in the developer solution, and a polar group (HAMA) to improve the adhesion of the film to the substrate.

The 248nm photoresist (fig 13a) typically contained benzene rings that improve the PR resistance to etch processes. However, these structures strongly absorb the 193nm irradiation and therefore, the photo-catalytic reactions at such low exposition wavelengths were not efficient. Thus, lithographers moved towards acrylate based polymers which do not absorb the 193nm wavelength (Fig 13b). These photoresist contain different monomers, each of them with a specific function, such as, C-rich *protective groups* to improve the PR thermal stability, *lactone groups* to improve the PR solubility in the developer, or *polar groups* for adhesion enhancement. However, they are more sensitive to plasma etch processes due to the absence of benzene groups in the polymer chain. Besides, to avoid pattern collapse or ARDE issues in small PR patterns, the lithography tends to reduce the deposited photoresist thickness.

However, this strategy is not sufficient to ensure proper pattern definition for the latest CMOS technologies. **Another option to further improve the resolution is increasing the numerical aperture (NA)** or in other words, working in an environment whose refractive index is higher than 1 (n>1). Thus, from the 45nm technological node, *immersion lithography* where lithography scanners are submerged in a water environment (n= 1.44) have been introduced to improve the resolution.

Since then, the immersion lithography has reached its limitations and the dimension reductions with this technique have been at a standstill. Therefore, other lithography strategies such as Extreme UV lithography [42] or e-beam [43] lithography are under development. However, these strategies being expensive and not mature at this moment, **to improve the gate pattern resolution, most companies use double patterning strategies at least until the 14nm technological node.**

The double patterning process enables to double the pattern density from a conventional 193nm immersion lithography step. The main advantage of this technique is that it enables the definition of structures beyond resolution capability of existing lithographic tools without drastic changes in manufacturing infrastructures. There are two main types of double patterning technology: pattern-splitting type such as Litho-Etch-Litho-Etch process (LELE) [44] and self-aligned double patterning (SADP) [45].

At ST Microelectronics, the LELE approach is used. It consists in the definition of the gate pattern in two steps using a litho-etch-litho-etch (LELE) approach. In a first step, referred as GATE etch, a first resist pattern (typically composed by gate lines) is transferred into the HM stack (Fig I.15).

Then a new lithography stack is deposited over the already patterned HM layer and a second lithography is done with a different mask design (Referred as CUT). This second lithography is used to cut the gate lines in different positions. Combination of both lithography patterns will define the final gate 2D patterns which are then transferred into the full stack.

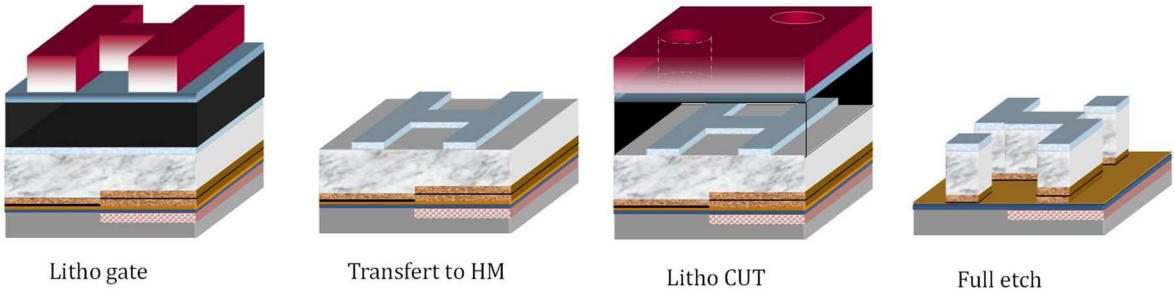


Figure I-15 Double patterning process: a first lithography step is used for gate pattern definition which is transferred to the HM layer. Then, in a second lithography step, the CUT definition is carried out. This new mask is used to cut the gate lines at certain points and define the final gate pattern at the HM layer. Finally, the gate pattern is transferred into the full stack.

I.4.1.2 Sensitivity

The photoresist sensitivity is its efficiency to undergo photo-catalytic and deprotection reactions under UV exposure. For example, a very sensitive photoresist will undergo many photo-catalytic reactions under low UV expositions. In other words, a lower UV *dose*, or the amount of UV irradiation per cm^2, is required for resist exposition. Working at lower doses is advantageous because it results in a reduction of the exposition time and therefore allows increasing the *throughput*, or the amount of processed wafers. Besides, at lower doses, a better control of the deprotection reactions can be obtained which can improve the pattern resolution.

To further improve the photoresist sensibility, chemists play with the polymer and PAG compositions to obtain more sensitive photoresists. For example, they will choose polymers with lower activation energies for the deprotection reactions (lower PEB) so that they react more easily with the PAG acids. Thus, we will be able to reduce the PAG concentration within the resist film and therefore, reduce the acid formation. This allows a better control of the deprotection reaction and limits the diffusion of the acid groups towards the non-exposed photoresist patterns. Due to these modifications, the photoresist chemistry has strongly changed. The first 193nm photoresist generation consisted in simple methyl methacrylate based polymers with only three different monomers [46]. Today, the 193nm photoresist present really complicated chemistries with 6 or more different monomers. This means that moving towards more sensitive photoresist may become a challenge for plasma etch processes.

I.4.1.3 Roughness

The Roughness is an irregularity on the pattern line edge that results in variations of the average gate dimension or Critical Dimension (CD). To characterize the pattern roughness two parameters are used, the Line Width Roughness (LWR) that represents the CD standard deviation along an “infinite” line; and the Line Edge Roughness (LER) that represents the line edge variations.

$$LWR = 3\sqrt{\sum_{i=l}^{n}\frac{(CD_i - \overline{CD})^2}{n}} \quad LER = 3\sqrt{\sum_{i=l}^{n}\frac{(x_i - \bar{x})^2}{n}}$$

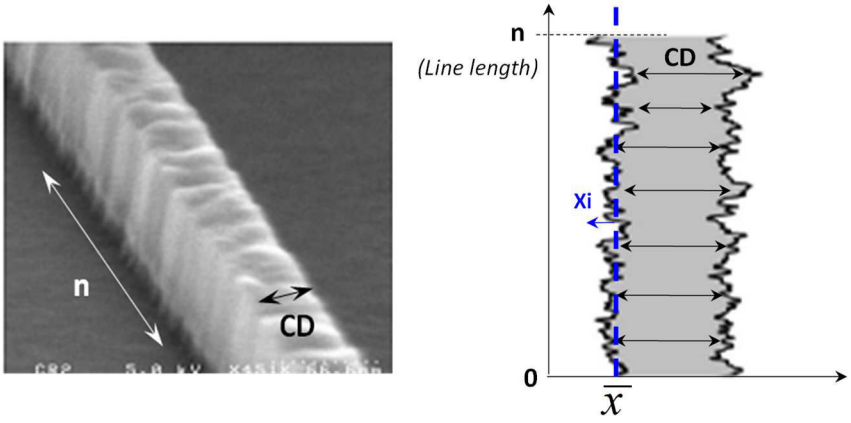


Figure I-16 Schematic representation of roughness parameters: LWR and LER.

The line's right edge and left edge roughness variations can be correlated, not correlated or anti-correlated. An illustration is shown in Figure I.17.

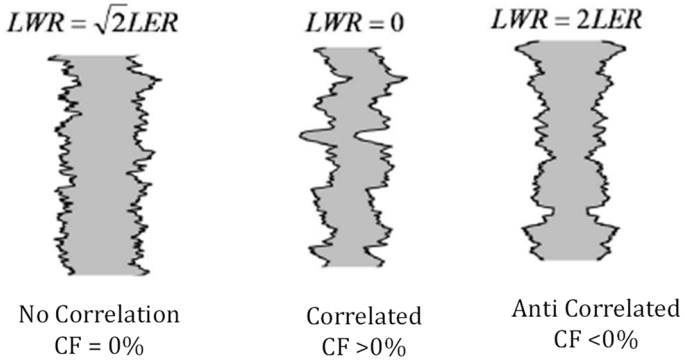


Figure I-17 Schematic representation gate patterns with no correlation, correlated sidewalls and anti-correlated sidewalls. CF refers to Correlation Factor.

The correlation degree between both line edges is defined by the correlation factor (or correlation coefficient, ρ), which is given by:

$$\rho = \frac{{\sigma_L}^2 + {\sigma_R}^2 - {\sigma_{CD}}^2}{2\sigma_L\,\sigma_R}$$

Where, σ_{CD} is the standard deviation of the line width and σ_L ,σ_R, are the standard deviations of the left and right edges, i.e. the LWR, LER left and LER right respectively. The correlation coefficient can vary between -1 to +1. When the left and right edges of the patterns are uncorrelated (i.e. if the edge positions are independent from each other), the LWR and the LER are related by $\sigma_{LWR} = \sqrt{2}\sigma_{LER}$, resulting in a null correlation factor. The correlation coefficient is positive when the edges are correlated (i.e. when they tend to follow each other in phase which corresponds to wiggled patterns). If they are perfectly correlated, $\rho = 1$ and then, $\sigma_{LWR} = 0$, even if $\sigma_{LER} \neq 0$. The correlation coefficient is

negative when the edges are anti-correlated, i.e. when they tend to follow each other in opposition of phase. In this situations, the LWR and LER are related by LWR = 2LER.

The origin of the photoresist LER is attributed to many contributors, such as, the lithography mask roughness [47], the resolution (i.e. the contrast between the exposed and un-exposed PR patterns) [48], the "shot noise" (i.e. the statistic variation of the applied dose) [49] or the acid diffusion within the un-exposed photoresist pattern [50] [51].

Unfortunately, all these contributors are correlated and it becomes complicated to find a good compromise to reduce the PR LER but keeping a good pattern resolution and PR sensibility. For example, by increasing the acid diffusion length, the LER can be improved. However, if the acid diffuses too much within the PR film, then, the resolution will be degraded ref. The same occurs if too sensitive resists are chosen. In this case, the dose needs to be reduced to keep a good resolution, but at low doses, due to the shot noise effect, the LER is degraded. To improve the LER either we work at high doses, or we increase the acid diffusion, but both degrade the resolution. In conclusion, there is no way to improve the Sensitivity (i.e. dose reduction) and the resolution (i.e. pattern definition) keeping low LER values. This is described as the "*lithography incertitude principle*" (i.e. LSR principle) and resumes the challenges to find a good compromise between Sensibility/Resolution/LER.

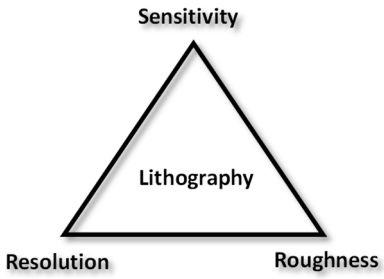


Figure I-18 Lithography incertitude principle

Along with downscaling, finding a good compromise becomes more and more challenging because, to pattern small gate designs, extremely sensitive photoresist are required, which supposes a problem in terms of pattern LER degradation.

Besides, the increasing pattern density and the mask design complexity make of pattern resolution a very critical point. For example, in the logic integrations of the latest CMOS devices, we can find 2D gate structures that are not easy do define at the lithography level. Some examples are shown in Figure I.19.

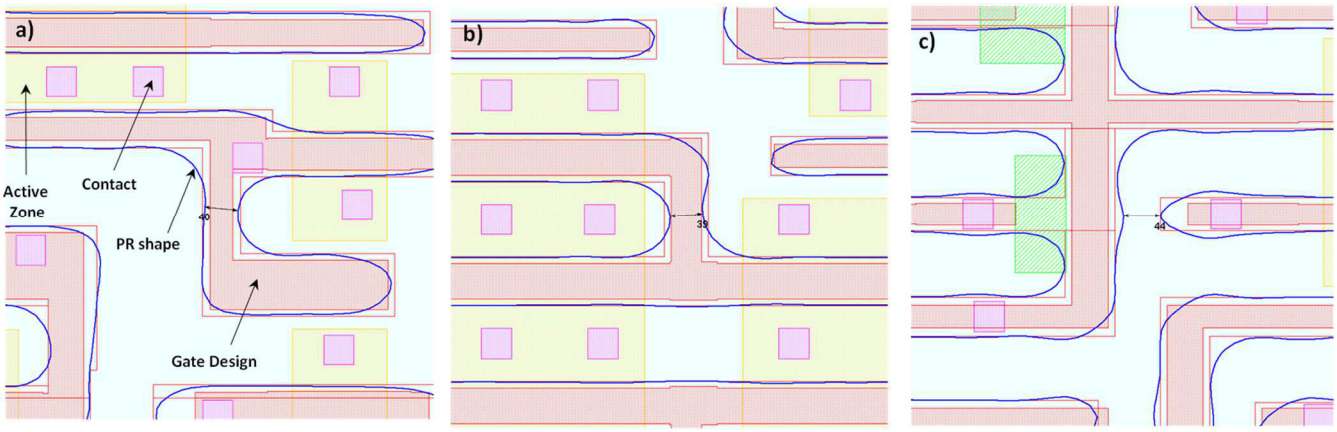


Figure I-19(a, b & c) Three examples of 2D structures designed for the latest logic CMOS technologies. The gate designs are represented in red. Pink squares represent contact position while orange and green squares represent the active zones. The photoresist pattern shape is illustrated by the contour defined by the blue lines. To better identify the PR pattern shape deformations, the resist profile and the designed structures are overlapped.

Due to resolution problems U-Shape structures are not patterned with a good fidelity (i.e. rounded corners, short line ends….). To improve the pattern definition, the lithography benefits of the "Optical Proximity Correction" (OPC) models which correct and modify the mask design considering the lithography pattern deformations in order to improve the PR pattern definition [52] [53]. However, even with the addition of all the lithography corrections, the definition of small gate features still remains a challenge in some gate integrations.

I.4.2 Challenges related to the dry etch processes

Gate etching itself is also a very challenging process because, perfectly anisotropic gate profiles need to be patterned over gate stacks comprising a wide number of different materials. **Thus, an etch process needs to respect five criteria: a good anisotropy, strong selectivity, CD control, etch rate uniformity and low damage.** Considering the ITRS specifications for the latest CMOS technologies, these criteria become more and more difficult to respect.

- **Anisotropy:** In the gate etch processes, perfectly anisotropic (vertical) gate profiles need to be obtained without impacting the selectivity or damaging the underlying layers. For this, the ion bombardment as well as the deposition and etch mechanisms need to be controlled at a nanometer scale.

- **Selectivity**: The etch selectivity is the etch rate ratio between the etch rate of the etched material relative to that of the masking material or the underlying layer.

$$S = \frac{ER_{\text{etched material}}}{ER_{\text{underlying material}}} \qquad \text{(Eq. I.4)}$$

  Ideally, the selectivity should be infinite or at least >>1. A good selectivity is extremely important because usually the etch processes need to be stopped on ultra-thin layers. For example, in the case of the HfO_2 HK etching, the process has to be stopped on the underlying silicon where the source and drains will be elaborated, without consuming or damaging it. These processes are often carried out in BCl_3/Cl_2 chemistries. As it will be explained in Chapter II (section II.2.2.3), BCl_3 addition improves the selectivity because in presence of silicon it

initiates a BCl_x deposition process that stop the silicon etch reaction. By this way, an infinite selectivity is obtained [54].

- **Low Damage**: This means that the plasma processing must leave intact the underlying surfaces without any amorphization, defect generation, or silicon recess… For example, initially, for the gate patterning process, the polysilicon was etched using a HBr/O_2 chemistry that is extremely selective to the underlying gate silicon oxide (i.e. in classic MOS integrations). However, after long over etch steps, due to the formation of diffusion channels, the underlying silicon can be oxidized and be removed by wet solutions, which results in silicon recess issues [55]. Another example is the damaging of polysilicon layers under exposure to strong VUV irradiation, which results in the creation of defaults that are detrimental for the device performances [56]

- **Etch rate uniformity**: For an etch process to be industrially applicable, high etch rates are required in order to increase the throughput. However, if the etch rate is too fast, it becomes complicated to control the process during thin film etching. Besides, it should be considered that due to the presence of nearby reactor walls, for example, the etch rates present typically a center-edge non-uniformity which is not always easy to control.

- **CD control:** with the CMOS downscaling, the requirements in term of CD control become even more stringent. The CD uniformity must be controlled at less than 10% of the targeted CD. This uniformity comprises the variability from lot-to-lot, from wafer-to-wafer**,** and within the same wafer [57]. Concerning the 14FDSOI integrations, the targeted gate CD is ~20nm, with a CD uniformity of 2nm.

The LWR/LER can also be considered as a parameter of the CD control since it is the variation of the CD along the same gate length. To ensure good electrical performances of the devices, the ITRS recommends that the LWR should be controlled at less than 12% of the targeted CD, which corresponds to a LWR of 2.4nm over 20nm gate lines. In fact, several experimental and modelling studies indicate the harmful effects that LER or LWR may have on the voltage threshold shift (due to the variations of the conduction channel length) [58], or the off-state leakage current in a typical MOSFET [59]. Therefore, sidewall roughness becomes one of the biggest concerns for the gate patterning process. The lithography strategies are today not enough performing to reduce the photoresist sidewall roughness, meaning that etch strategies have to be implemented.
In this work, the main focus was to answer to the CD control criteria and more particularly to control the gate's line width roughness in advanced HGKM gate patterning for 14FDSOI technologies.

I.4.3 Lithography & Etch: A Combined Interaction

With downscaling, the interactions between the lithography and etch processes are no longer negligible but instead become critical. In the previous section, we have said that our goal is to reach the criteria on CD control and LWR. Therefore, in this section we will discuss about the combined interaction of lithography and etch processes on these two variables.

I.4.3.1 CD Control

It is well known that the lithography process modifications impact the gate etch processes. For example, as previously explained in section I.4.1, the lithography needs to increase the throughput and the

resolution, and this requires shifting towards more sensitive photoresists with lower deposited thickness. This implies that, during the etch process, the PR will be very sensitive to the plasma processing which results in a reduced selectivity and resist budget issues. These issues impact the photoresist profile during the etching process and therefore, the gate stack profile is also affected. For example, we could imagine the formation of tapered gate profiles due to photoresist lateral erosion (see I.3.2.2).

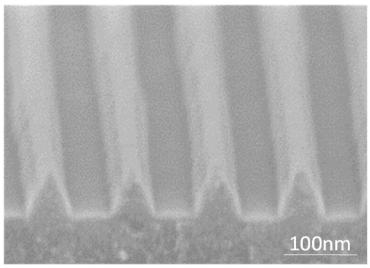


Figure I-20 SEM Cross section image of a photoresist pattern lateral erosion during the SiARC etching step

In addition, along with the gate pattern miniaturization, the pattern density and complexity increases. In the latest mask integrations it is quite common to find dense structures with random 2D gate features that are not easy to pattern. This becomes particularly challenging for gate-to-contact patterning processes (Fig.I.21). In such processes, as shown in Figure I.5, first the gate patterns are defined and then in a second patterning step (litho + etch), the contact patterning is carried out. For this, extreme metrology is required to make sure that both lithography masks (for gate and contact feature definition) are well aligned and that the contact patterns are perfectly placed over the gate structures or source and drain zones. Thanks to the use of advanced lithography metrology techniques, the gate-to-contact alignment can be well controlled at the lithography level. However, the presence of dense 2D random patterns in the integration of gate designs, and the difficulty to etch small contacts between the gates, makes of this stage one of the most challenging ones in terms of gate patterning (Fig I.21). Thus, it seems clear that for the latest nodes, we need to be able to etch small gate patterns with an extreme anisotropy and strong pattern fidelity.

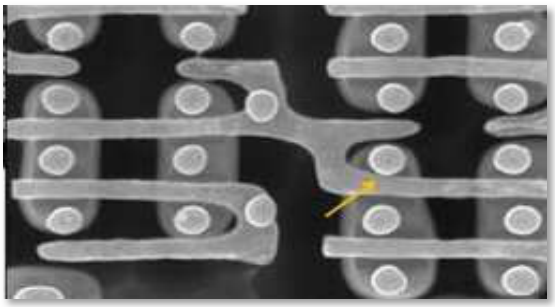


Figure I-21 SEM image of a 2D gate structure after contact etching. The difficulty to etch small contacts and the complexity of gate designs makes of gate patterning a very challenging process. The small gate to contact space margins are illustrated by the yellow arrow.

However, we can also find some studies that prove that the etch process steps also impact certain parameters typically attributed to the lithography processes. For example, *Gatefait et al* claimed that the wafer overlay margin (i.e. the alignment between different lithography levels, i.e. the contact-to-gate alignment) is modified along the gate etch processes [60]. Other studies affirm that the gate etch steps can modify the gate features. For example, *Gu et al* proposed resist consumption and internal stress build-up during resist trimming leads to resist line bending and pattern deformation [61](Fig 22a).

Other resist deformations were also reported by *Wallow et al*, who claimed that photoresist undergo volume shrinkage under exposure to 172nm UV light [62]. This results in photoresist pattern deformations such as line edge pullback and elbow or corner displacements (Figure 20b).

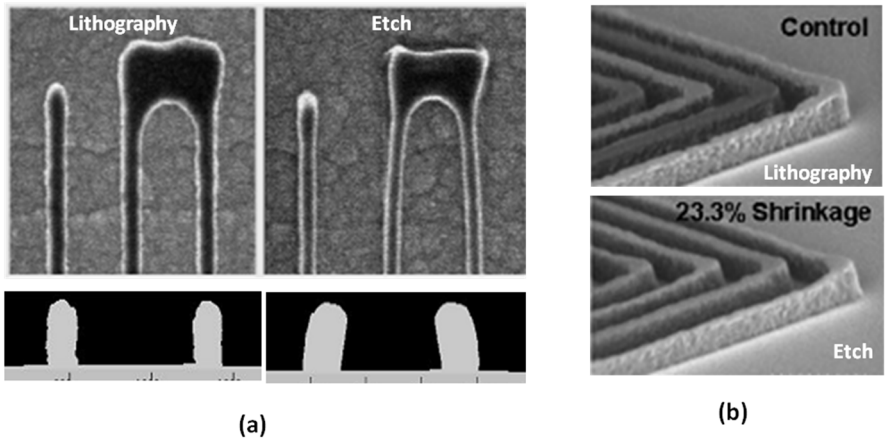


Figure I-22 Examples of gate pattern deformations during gate patterning process. (a) The photoresist patterns are deformed during long trim steps leading to a 2D pattern deformation [61]. (b) Other studies report the shrinkage of photoresist patterns under UV curing [62].

In addition, *Szucs et al* also proposed a new OPC model to correct the lithography masks considering the pattern deformations occurring at both, lithography and etch processes [63]. And finally, the most well known example is the local gate CD non-uniformity (i.e. LWR and LER) modifications during gate etch processes. Though the origin of the LER stands on the lithography process, many studies support that the PR LWR can be degraded during the gate etch process (i.e. due to bad PR/SiARC selectivity, strong ion bombardment…) [64]. This is further discussed in the following section.

I.4.3.2 Roughness (LWR and LER)

As previously explained, the roughness is a subject of great concern because it directly impacts the electrical performance of the integrated circuits [59] [58]. Though many efforts have been done at the lithography level to improve the PR LWR [65] in the best lithography conditions, an LWR of 4-5nm is obtained. Considering that gate patterns critical dimension is ~20nm, a roughness of 4-5nm supposes 25% variation of the averaged CD value. The ITRS specifies that the LWR should not exceed 12% of the CD length which is still far from the state-of-art process. Besides, this roughness may be further degraded during the etch processes. Previous studies show that the most critical steps are those used for the hard mask patterning where the photoresist material is still present at the top of the gate stack [66] [67]. **In fact, due to the poor etch selectivities, and the weak photoresist resistance to etch processes, the resist patterns are strongly degraded during plasma processing. This degradation results in an increased LWR that is transferred along the gate stack.** However, once the hard mask has been structured and the remaining photoresist is removed, the pattern degradation is reduced and the HM LWR is mostly directly transferred into silicon.

To improve lithography performances, post-lithography treatments such as plasma cure treatments have been introduced [66] [17]. The interest of adding such cure steps is that they not only improve the PR sidewall roughness after the lithography process but also improve the PR resistance to etch processes. Therefore, they improve the LWR but also, the CD uniformity and photoresist selectivity.

The first studies carried out concerning the photoresist pretreatments were presented by *Mohorowala et al* and consisted in HBr cure treatments used for resist reinforcement [68]. As it was observed, the photoresist chemical functions containing oxygen atoms are removed during the HBr treatment which improves the etch resistance on the resist material [68]. However, the mechanism leading to such reactions was still not well understood.

It was in a latter report presented by *Pargon et al* and *Bazin et al* that the main contributors for the oxygen removal reactions were identified. In their work, they could isolate the plasma UV contribution from the plasma species (radicals and ions), and they observed that, the chemical modifications of the photoresist are intimately linked to the UV plasma emission at λ<200nm [69]. The amount of reactions that occur within the polymer depends on the UV penetration depth. For wavelengths of λ<200nm it is known that these chemical modifications occur within the whole PR volume [70]. Based on FTIR analysis, they evidenced that, under UV exposure, there is a preferential cleavage of the C-O-C and C=O bonds due to the photolysis of ester and lactone groups present in the PR into CO and CO_2 volatile species. Such ester groups link the functional lateral groups to the polymer main chain and therefore, their decomposition results in the detachment of lateral groups which may remain within the photoresist film as plasticizers or are released into the gas phase [71]. This leads to an increase of the polymer free volume that allows polymer chain reorganization leading to more densified PR patterns with lower surface roughness [72] [17]. **Therefore, the VUV emission during plasma treatments is responsible of the photoresist smoothening mechanisms. However, the carbon rich molecules released from photolysis reactions are dissociated in the gas phase to form non-volatile carbon radicals that can redeposit over all surfaces exposed to plasma [73]. This deposit forms a dense carbon crust over the PR pattern that prevents pattern from deformation (Fig I.23).**

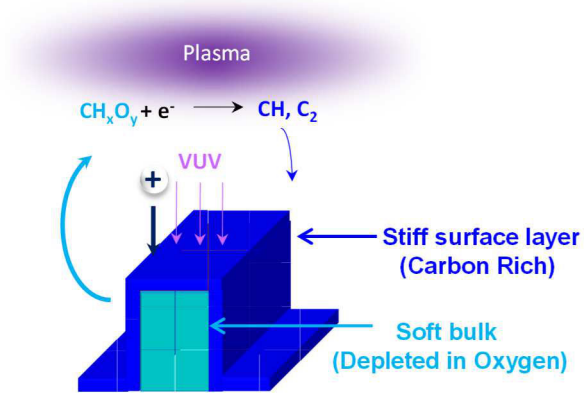


Figure I-23 Schematic illustration of the photoresist cure mechanism

Previous studies carried out by *Azarnouche et al* [17] [74] showed that VUV cured resists present more rounded, and reflowed patterns as compared to HBr cured photoresists (Fig I.24). According to their findings, VUV induced chain scission induces a drop of the resist glass transition temperature (Tg) that promotes resist reflowing. The formation of a graphitized layer on PR pattern sidewalls prevents the resist reflowing therefore maintaining square resist profiles.

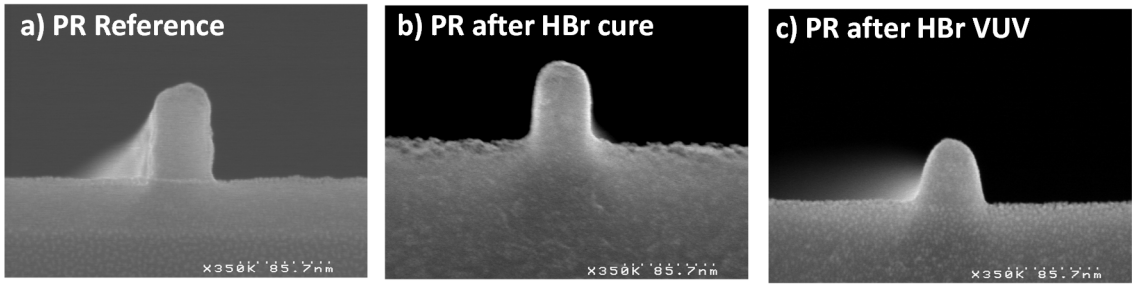


Figure I-24 SEM observation of Resist pattern: (a) after lithography, (b) after HBr plasma treatment, (c) VUV light treatment [17][80]

However, the mechanical differences between the stiff surface layer and the underlying soft resist bulk result in a stress formation within the PR pattern. **The stress relaxation of the hard surface layer onto the soft PR bulk generates surface buckling which degrades the resist roughness [75] [76] [77]. Previous studies have shown that decreasing the thickness of the deposited carbon layer contributes to the reduction of the buckling amplitude [76] [75]. Therefore, the strategies for LWR minimization consist on searching for plasma conditions that emit an important VUV flux but limit the carbon re-deposition.** For example, in the literature, many different plasma chemistries have been studied, such as, HBr, H_2, Ar, He or HBr/O_2 processes [66] [78]. Between them, H_2 and HBr/O_2 plasma processes result in the best LWR of around ~3nm. This is related to the chemical reactivity of hydrogen and oxygen species that prevent from carbon deposition.

However, if such strategies allow meeting the CDU and LER requirements for the 32nm technological node, it is no more efficient to address the specifications of the latest CMOS. After photoresist pretreatment, the best results that can be obtained are a LWR~3nm, still remains high as compared to the ITRS specifications (LWR of 2.4nm). Other strategies need to be found to further decrease the gate LWR.

I.5 Objectives of this work

There are many studies that illustrate the interactions between the lithography and etch processes. In particular, the pattern definition and pattern roughness are no longer only dependent on lithography step but are also impacted by etch processes. Therefore a combined effort of both; lithography and etch engineers, is required to successfully carry out the gate patterning process. So far, many efforts have been done to improve the gate patterning process in terms of pattern uniformity, fidelity and LWR. However, there are still some aspects that have not been studied yet.

For example, most studies are focused on the patterning of dense or isolated gate lines using photoresist-cure steps to improve the pattern transfer process. However, few people have looked at the evolution of 2D gate patterns during the gate etch process. Yet, these features are the most challenging to define for the lithography process and it is important to verify if the gate etch process modifies the definition of 2D gate structures in our process conditions. Besides, much work has been done to improve the PR roughness at the lithography level [65]or by addition of cure steps [66]. The LER transfer into simple polysilicon gate stack is also well reported [67]. However, these studies show that the bare addition of cure steps is not enough to reduce the LER sufficiently to meet the specifications defined by the ITRS.

The goal of this work is to bring answers to the CD control and roughness transfer mechanisms in complicated real 14FDSOI gate stacks. This includes the analysis of the CD evolution over

complex 2D structures and the LWR evolution all along a gate stack including the HKMG ultra-thin layers. This requires the use of adapted metrology and a methodology that will be described in chapter II.

To meet our goals, we have worked on three main axes: the impact of cure steps (Chapter III), the masking strategies (Chapter IV), and the impact of the gate stack itself (Chapter V). The interest of this work is to determine the main contributors for the LWR generation during a gate patterning process and to evaluate if the HKMG etch steps modify the final gate patterns and LWR.

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Chapter II. Experimental Set up

In this Chapter, we propose a description of the main techniques used for substrate preparation and process characterization. First a description of the gate patterning process and the gate stack is presented. Then, the equipments and processes used for sample elaboration are briefly described. This includes a description of the deposition and etch reactors and the description of the gate etch process conditions. Finally, to better understand the results presented in the following chapters, the operating principle of the most relevant characterization techniques is detailed. This includes: several material characterization techniques (FTIR, TGA, XPS and XRD) and the description of the strategies used for the gate CD and roughness metrology (CD-SEM and AFM metrology).

II.1 The gate patterning process

The experiments were carried out over standard 14FDSOI gate samples. To better understand the sample elaboration process, a schematic representation of the 14FDSOI gate patterning process is shown in Figure II.1.

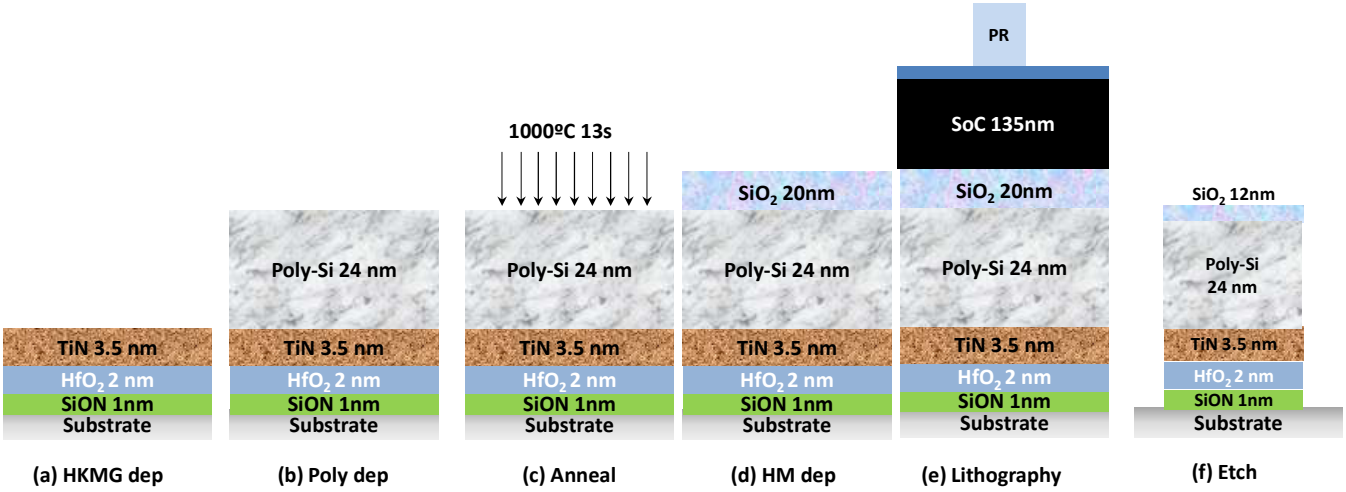

Figure II-1 Gate patterning process schematic description: a) HKMG deposition (SiON, HfO_2 and TiN), b) polysilicon deposition, c) Source-Drain Anneal, d) SiO_2 hard mask deposition e) Tri-layer deposition and lithography and f) Dry etch. This process flow concludes with a wet clean step in HCl/HF for polymer removal. (The stack drawings are not scaled)

After preparation of the 14FDSOI substrate (i.e. active zone and isolation trench formation) the HKMG stack composed of a thin TiN metal film of 3.5nm deposited onto a HfO_2 High-K layer of 2nm is deposited using RF-PVD (for TiN) and ALD (for HfO_2) deposition techniques (Figure II.1a). Afterwards a 24nm polysilicon film is deposited by CVD (Figure II.1b) and annealed at 1000°C for 13s to allow dopants (As, B…) to diffuse into silicon (Fig II.1c). Then, the 20nm SiO_2 hard mask is deposited by CVD

(Fig II.1d). To conclude, the lithography tri-layer stack is deposited. This includes a 193nm photoresist, the "SiARC" anti reflective coating and the "SoC" amorphous carbon planarizing layer deposition. The gate stack is then exposed in an immersion lithography cluster to define the desired gate patterns into PR films (Fig II.1e).
In a second stage, the lithography defined patterns are transferred into the full stack with suitable dry etch recipes in an ICP etch reactor (Fig II.1f). To finish, the gate patterns are cleaned using HF/HCl acid mixtures in a wet etch step to remove residual polymers and oxide passivation layers.

Finally, it should be noted that, in our process conditions, the masking strategy (i.e. SiO_2 HM) slightly differs from the one used for the 14FDSOI node at STMicroelectronics. In fact, due to several modifications in the manufacturing process, the 14FDSOI gate designs are carried out with a dual HM composed of a 28nm SiO_2 oxide layer deposed over a 28nm Si_3N_4 nitride layer. A comparison of the standard 14FDSOI gate stack and the gate stack chosen for this work is shown in Figure II.2.

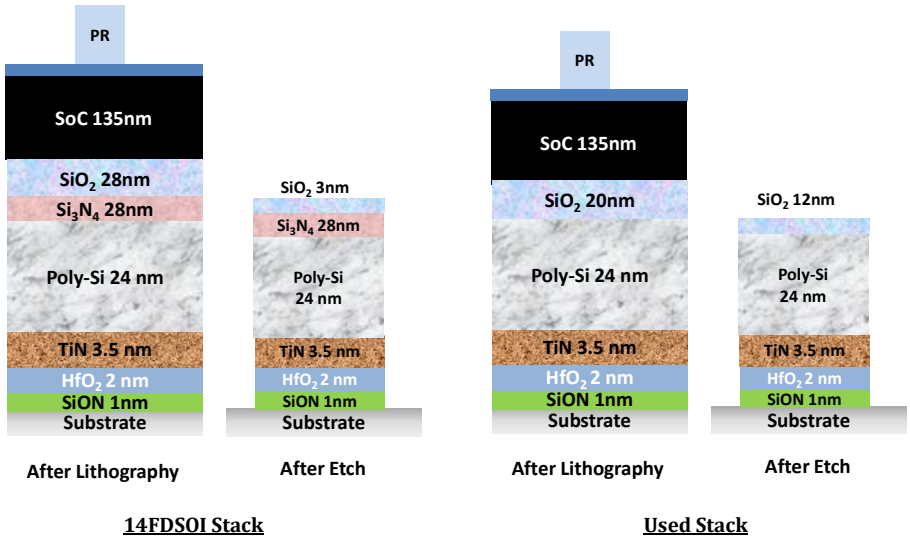

Figure II-2 The 14FDSOI gate stack compared to the gate stack used for this PhD work. The full gate stacks are illustrated before and after full etch.

As it can be observed, for the 14nm node, really complicated gate stacks are developed. This requires the use of specific manufacturing techniques with complicated process conditions. In the following section, a description of the main deposition and etch techniques is presented.

II.2 Equipments for gate patterning: Deposition and Etch reactors

As previously explained in section II.1 many different deposition techniques are used for the elaboration of the full gate stacks (i.e. ALD, CVD, PVD…). However, from all the deposited films, the TiN metal layer is of relevant importance because it is the core of the HKMG transistor and is the responsible of the electrical functionality of the designed devices. Therefore, in this PhD, a special attention is paid to the TiN film deposition conditions and their impact on the gate patterning and the final gate LWR.

As a result, in this section, only the Applied Materials Endura RF-PVD reactor used for TiN deposition and the LAM Ex ICP reactor used for the gate etching processes are described. The RF-PVD deposition processes were carried out in collaboration with C. Suarez, PhD student at STMicroelectronics, while the etch processes were carried out by myself.

II.2.1 The Endura RF-PVD TiN deposition reactor

II.2.1.1 The RF-PVD principle

The Radio Frequency Physical Vapor Deposition (RF-PVD) is a deposition technique that was developed for the deposition of metal gate layers without damaging the insulating layers deposited underneath.

This method is based on the same principle as a Plasma Enhanced Physical Vapor Deposition process (PE-PVD) where metal atoms are sputtered from a target material by ionic bombardment generated by the presence of a nearby plasma.

In practice, within a low pressure reactor, a gas (typically Argon) is ionized due to the addition of an electric field which leads to the formation of energetic electrons and Argon ions [1].

$$Ar + e^- \rightarrow Ar^+ + 2e^-$$

Due to this electric field the electrons are accelerated towards the anode (i.e. substrate) while the positive ions are accelerated towards the cathode (i.e. target). This results in the sputtering of the target material (i.e. metal) and the release of metal atoms within the gas phase. The ejected atoms will then pass through the generated plasma and deposit over a substrate. A schematic illustration of the deposition process is shown in Figure II.3.

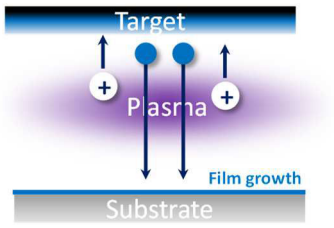

Figure II-3. Schematic illustration of the deposition process

Most of the PVD deposition techniques are carried out using a continuous magnetron direct current discharge for the plasma ignition and target sputtering. In these conditions, to create a discharge between two electrodes, an important electric field is required that exceeds the breakdown tension (V_b) or the minimum tension required for plasma ignition. This potential depends on the ionized gas (i.e. Argon), the working pressure and the distance between both electrodes. However, to reach the breakdown tension, high potentials are required which result in the formation of energetic electrons that are accelerated towards the anode and can damage the substrate material (i.e. HfO_2) [1].

To avoid these disadvantages, the RF-PVD discharges were developed. This consists on the superposition of two source powers, an RF power that will ensure the plasma ignition, and a DC magnetron tension that controls the ion energy and the target sputtering. This permits to control separately the plasma ignition and the ion energy, and therefore allows working at lower power conditions, and typically lower working pressures. Besides, since lower source powers are required for plasma ignition, the generated electrons have lower energies and therefore induce lower damage in underlying HfO_2 HK layers [1] [2].

II.2.1.2 The Experimental Set-up

The TiN depositions are carried out in an Endura RF-PVD reactor from Applied Materials. This equipment has 4 different chambers that allow the deposition of different metallic materials (Ti, Al, Ti-Al Alloys and La). The system is also equipped with hot plates that allow wafer out-gassing before and after metal film deposition.

All the chambers are pumped to a secondary vacuum and can reach a minimum pressure of $5x10^{-5}$ mTorr. During deposition, the gas flow can be adjusted between a range of 0 and 150sccm. The chamber working pressure is also controlled by an adjustable valve and can vary between 1 and 25mTorr. To avoid damaging the FDSOI substrates, thermal budget for HKMG layer deposition is limited [3]. Therefore, all the metal depositions are carried out at a wafer temperature of 20ºC. To ensure wafer thermalization, the wafer is placed over a support with an electrostatic chuck that is cooled down by a heat exchanger. An argon backside flow is also added to allow a proper thermal transfer between the support and the wafer. The reactor walls and the target materials are also thermalized by the circulation of a deionized water flow.

However, for really long deposition times (>2min), the sputtered metal atoms are cumulated over the target and the reactor walls, and form thick deposition films that get heated during the process. This may lead to a detachment of the excessive deposition that is re-deposited over the wafer forming particles that are killer for the ICs. Therefore, to avoid excessive heating of chamber walls and target materials, the maximum deposition time is fixed to 100s, after which the DC and RF powers are stopped for 4-5 seconds to allow chamber cooling. This process is referred as a deposition cycle. Therefore, for the deposition of thick metal films subsequent cycle repetition is carried out [2].

A Schematic representation of the RF-PVD reactor used for TiN deposition is shown in Figure II.4.

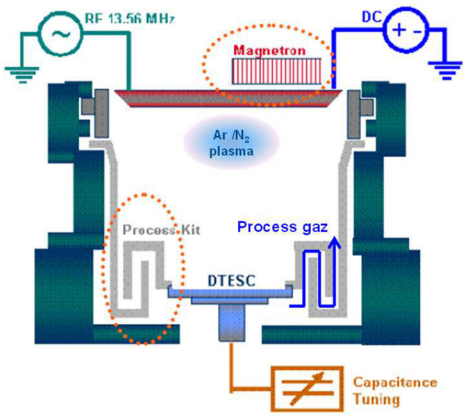

Figure II-4 Schematic representation of the RF-PVD reactor

II.2.1.3 Deposition of TiN films by RF Physical Vapor Deposition (RF-PVD)

For TiN deposition, Ti targets are sputtered in a chamber where the plasma is generated by an Ar/N_2 gas mixture. The nitrogen is dissociated within the plasma and results in free radicals that react with Titanium and deposit TiN films. Clearly, the addition of nitrogen species to the plasma can significantly modify the discharge parameters and strongly influence in the grain formation mechanisms.

In general, to modify the morphology of the deposited film we will most likely modify plasma conditions by changing the RF power and working pressure. In fact, the RF power impacts the plasma electron

density (n_e), while the pressure impacts the electron temperature (T_e). Therefore. By playing with these two variables, we can control the plasma dissociation and atom energy and consequently, the transfer of metal atoms towards the substrate surface. Besides, the substrate temperature also plays an important role on the grain formation mechanisms. It will influence the atom diffusion and promote the nitrogen or oxygen solubility within the TiN film [4] [5].

To better understand the relationship between the process conditions and the deposited film morphology *Thornton et al.* proposed a diagram that describes the film morphology evolution as a function of the working pressure and temperature (Figure II.5).

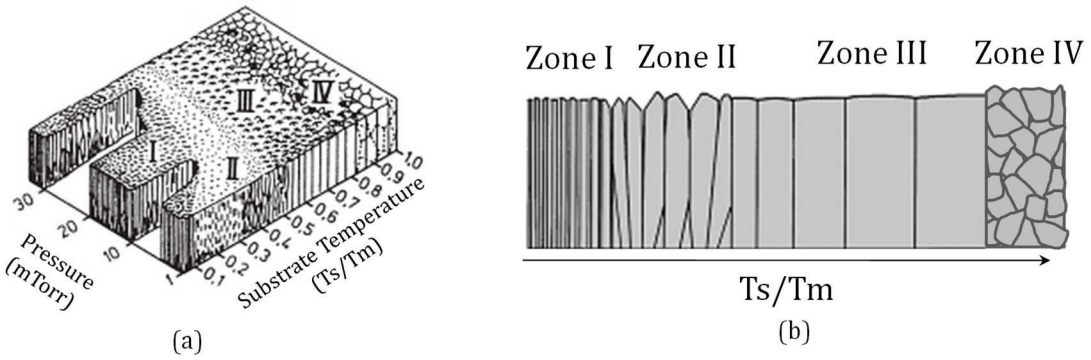

Figure II-5 Morphology of PVD deposited films as a function of the working pressure and substrate temperature [6] and a cross section illustration reprinted from *Petrov et al.* [7]*T* or T_s is the substrate temperature and *Tm*, the coating material melting point.

Where, *T* or T_s is the substrate temperature and *Tm*, the coating material melting point.

This diagram is divided in four zones. In Zone 1 (T/Tm<0.3) the grain structure is columnar, and consists in crystal grains defined by voided boundaries. In Zone 3 (0.3<T/Tm<0.5) the columnar grains are wider and are separated by well defined grain boundaries. Zone 2 (also known as zone T) consists in a transition zone between Zone 1 and Zone 3 where poorly defined fibrous grains are observed. Finally, in Zone 4 (T/Tm>0.5) the high working temperatures allows bulk diffusion and the formation of equiaxed grains.

In the standard deposition conditions, the TiN films are deposited at 600w (RF) and 700w (DC) source, low pressures (3mT) and low working temperatures (20ºC). Due to equipment limitations (i.e. no bias power available) and to avoid HfO_2 layer degradation, no substrate bias was applied. Therefore, the TiN film morphology should be similar to that of zone 1.However, it should be considered that the Thorton diagram illustrates the crystalline film growth at high film thicknesses (~50nm or higher). For thinner films, such as, the gate TiN film depositions (3.5-10nm), the films present a semi-crystalline-like structure where the TiN grains are distributed within an amorphous TiN phase [8].
A detailed description of the TiN growth mechanisms and the impact of the deposition conditions on the TiN morphology is proposed in Annex I.

In conclusion, a good control of the deposition conditions is of relevant importance because they can modify the film microstructure including its crystalline grain orientation or film surface roughness, which strongly influences the electrical properties of the deposited materials. **As reported by *Ohmori et al*, reducing the TiN grain size improves the electrical performances of the TiN metal gates** [9].

II.2.2 The LAM KiyoEx etch reactor

II.2.2.1 The Experimental set up

The etch processes were carried out in an industrial ICP KiyoEx reactor from Lam Research. The platform is composed of three different etch chambers (from which the Kiyo Ex is used for gate patterning) and a microwave chamber, used for in situ photoresist stripping.

In a Kiyo Ex reactor, the reactor walls exposed to plasma conditions are coated with an Y_2O_3 layer to avoid reactor degradation during processing.

The plasma is generated with a 13.56MHz RF generator placed at the top of the reactor over a quartz window. This allows delivering a source power between 0 and 1500W for plasma ignition. The RF source controls the ion density in the etch reactor (i.e. generation of high density plasmas of 10^{11}-10^{12}ion/cm^3 at low pressures). A separate control of the ion energy can also be obtained thanks to the addition of another13.56MHz RF generator at the bottom of the chamber (i.e. RF bias). This generator allows fixing the tension to a constant value within a range of 0-1200V and therefore controlling the ion energy.

The wafer is supported over a electrostatic chuck (ESC) that allows controlling the wafer temperature from 40 to 120ºC in four different wafer positions (i.e. inner center, outer center, inner edge and outer edge). The ESC is cooled down by a continuous flux of cold water (i.e. 10ºC). The temperature is finely tuned by controlling the power applied to resistances placed all over the chuck that will heat the wafer locally. The thermal contact between the wafer and the ESC is ensured by the addition of a backside Helium flow.

The gas injection can be carried out in two positions, at the center of the wafer or at the edge. Combinations of both is also allowed where the proportion of gas injected at each position (i.e. center/edge) can be controlled. The available gases for plasma etching are: $SiCl_4$, C_4F_8, NF_3, CO, HBr, CHF_3, CH_2F_2, Cl_2, O_2, He, SF_6, N_2, SO_2, CF_4 and BCl_3. The system is also equipped with an additional side tuning gas injection (STG) that consists in an injection of a CHF_3 gas at the wafer edge to improve non-uniformities. The pressure in the reactor is controlled by an adjustable valve that allows pressure regulation between 2.5mT and 400mT.

A schematic representation of the LAM KiyoEx reactor is shown in Figure II.6.

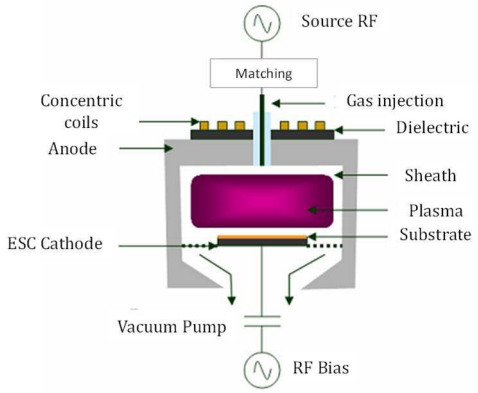

Figure II-6 Schematic representation of the Lam Kiyo Ex etch reactor

II.2.2.2 End point detection techniques (OES and LSR)

During the etch process, it is essential to determine with a good precision the end of each material's etching steps and the remaining material thickness. For this, the Lam EX reactor is equipped with an End point detection system that combines the techniques of Optical Emission Spectroscopy (OES) and Light Signal Reflectometry (LSR).

- **The Optical Emission Spectroscopy (OES)**

This technique is based in the spectral analysis of the plasma emitted light that allows to identify the reactive species present in the gas phase. In a plasma discharge, due to the interactions of electron and neutral species, the molecules are excited. During the relaxation process, light emission occurs. Each excitation state emits a specific wavelength (λ) and therefore, the molecules composing the plasma gas phase can be determined by analysis of the emission spectra. The light emission is collected by an optical fiber and detected by a CCD window that covers the spectral range between 200nm and 900nm with a wavelength resolution of 0.8nm. The intensity of an emitted ray can be followed by an adapted software and thus, thanks to the intensity variations we can determine the end of an etch process. For example, for silicon oxide etching typically the CO ray at 484nm is followed. At the beginning, the intensity of the CO ray increases, which is representative of the SiO_2 etching process. When all the silicon oxide is consumed, the intensity of the CO ray drops which indicates the end of the process (Fig II.7).

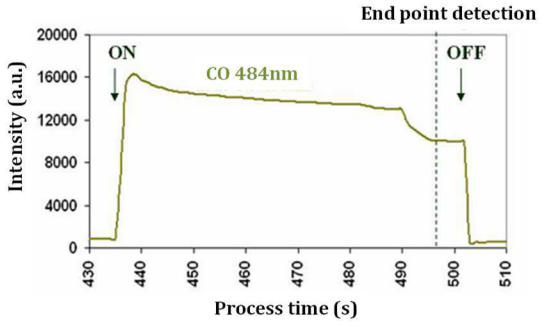

Figure II-7. Evolution of the CO 484nm ray intensity during a SiO_2 etching process in CF_4/CH_2F_2

- **Light Signal Reflectometry (LSR)**

To determine in real time the remaining film thickness the Light Signal Reflectometry is used. This consists on measuring the reflection of a monochromatic light beam that has been sent perpendicularly towards the substrate. The light is reflected by the different layers composing the substrate and due to the difference in the nature and the diffraction indexes of these layers, the reflected beam undergoes constructive and destructive interferences. These interferences depend on the material thickness and therefore, the remaining material thickness can be determined in real time. By this technique we can either determine the endpoint of a material at the interface with another material and also, we can stop the etch process before reaching this interface. As an example, Figure II.8 illustrates the endpoint detection of a TiN etch process Cl_2/CH_4 plasmas following the reflection of a 263nm incident light beam.

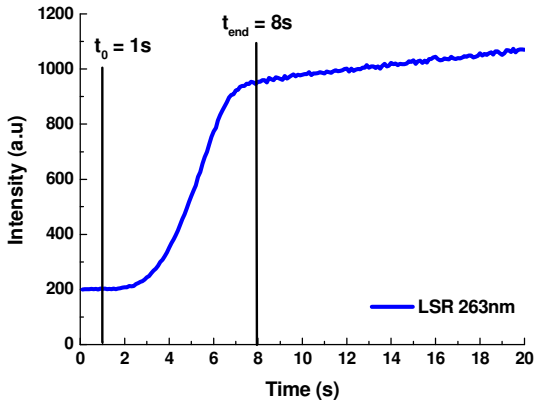

Figure II-8 TiN etch process in Cl_2/CH_4 plasmas followed using the reflection of a 263nm incident beam

The adequate use of these detection techniques becomes even more important when ultra-thin layers need to be etched with extreme precision. This is particularly challenging during the gate etch process, where several different materials need to be etched. In the following section, we will describe in detail the gate etch process conditions used at STMicroelectronics.

II.2.2.3 Gate etch process description

Typical gate etch process consists in a succession of the following steps: Lithography, photoresist cure, photoresist trim and subsequent material etch steps with selective plasma conditions. Figure II.9 shows a description of all process steps required for a 14FDSOI gate patterning at STMicroelectronics.

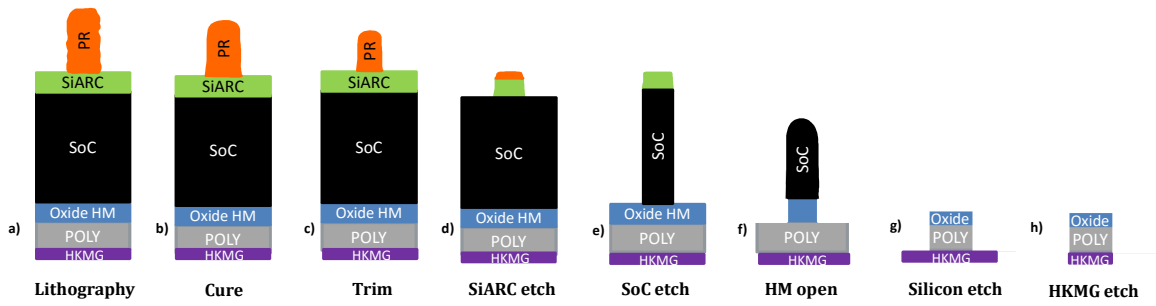

Figure II-9 Schematic representation of a gate pattern after: (a) lithography, (b) resist cure, (c) resist trim, (d) Si-ARC open, (e) SOC open, (f) hard mask open, (g) silicon etch, and (h) full etch.

Photoresists **pre-treatments or "Cure"** are VUV, plasma or thermal treatments initially implemented to modify polymer physico-chemical properties and increase photoresist stability to plasma etching . However, lately, the interest over these pre-treatments raised due to their ability to smooth photoresist sidewalls before pattern transfer (See Chapter I). HBr cure has largely been studied [10] [11], and is the candidate used in this study. However, many other pre-treatments have also been studied elsewhere such as; H_2, Ar or He [10], HBr/O_2 [12], or thermal pre-treatments [10].

Trim step consists here in Cl_2/O_2 plasmas that erode photoresist pattern isotropically to adjust pattern CD to target. These plasmas are purely chemical (no strong ion interaction). Other gases such as HBr/O_2 has also been studied [13]butCl_2/O_2 mixture is preferred in industry because its lower etch rate allows to control micro-loading and to improve iso/dense uniformity. In both cases, Oxygen is the main reactive species in the plasma and induces lateral etching of photoresist by forming volatile compounds like CO or CO_2. Chlorine or Bromine are basically added to limit lateral photoresist etch rate (ER) by formation of less volatile etch products like $C_xH_yCl_z$ or $C_xH_yBr_z$ that can redeposit on the photoresist sidewalls and decrease lateral etch rate.

The **Silicon Anti Reflective Coating (SiARC)** is a silicon based polymer (such as SiOCH) used in lithography to improve pattern resolution. Being similar to SiO_2, it follows the same etch mechanisms [14] [15]. Therefore, Si-ARC etch is carried out in fluorocarbon chemistry (CF_4/CH_2F_2/He). CF_4 will be the main etchant. It forms a CF_x type deposition layer that will provide the C and F precursors required to etch silicon oxide into volatile products such as SiF_2, SiF_4, CO and CO_2 [15].CH_2F_2 is added to increase CF_x deposition and create passivation layers to limit lateral photoresist etching.

Spin-on-Carbon (SoC) is a spin coated amorphous carbon (a-C) layer used to absorb the lithography irradiation and to flatten the surface. The plasma conditions for SoC etching need to be selective to SiO_2. At STMicroelectronics, SO_2/O_2 based plasmas are used where Oxygen will etch isotropically SoC and SO2 will limit SoC lateral etching or notching by a CS_x type deposition [16]. Other chemistries such as HBr/O_2 have also been studied [17]but have been replaced by sulfur based equivalents due to their poor selectivity towards photoresist and hard mask and their isotropy during SoC etching (no sidewall passivation).

Oxide Hard Mask (HM) opening is carried out in the same type of plasma chemistries as the SiARC etching inCF_4/CH_2F_2/He at high ion energies. In fact, to etch the SiO_2 HM a minimum ion energy is required to sputter the SiO_2 film and avoid excessive fluorocarbon deposition [18]. However, presence of some carbon deposition is also beneficial for oxide etching since it will contribute in the SiO_2 oxygen depletion by formation of CO and CO_2 volatile species which increases the oxide etch rate.

After this step, a **Strip** process in O_2 is carried out to remove remaining SoC and polymer residues.

Silicon etching is achieved in $SF_6/CH_2F_2/N_2$/He plasmas. The SF_6/CH_2F_2 plasma condition was chosen for its ability to improve micro-loading and polysilicon bowing (particularly in doped polysilicon gates) compared to other equivalents such as HBr/O_2 or $SiCl_4/Cl_2$ [19]. SF_6 is known for its ability to etch silicon and oxides leading to volatile products such as SiF_2 and SiF_4.CH_2F_2 was added to enhance sidewall passivation [20] [21]. In fact, by addition of such polymerizing gases the CF_3^+ ion formation is enhanced. These ions are neutralized at the silicon surface and form a CH_xF_y reactive layer on the silicon surface [22]. This fluorocarbon layer at the bottom of the structure is then sputtered due to ion bombardment and deposits over silicon sidewalls by a line of sight deposition mechanism forming a uniform passivation layer of ~1nm over the whole gate profile. Finally, N_2 contributes to the

equilibrium in the formation/etching of passivation layers by deposition of SiN_x type species or polymer etching forming CN_x byproducts [23].

The process ends by an **Over Etch (OE)** in HBr/O_2 also referred as soft landing. This condition was originally chosen for its increased selectivity to silicon oxide and TiN compared to other silicon etch chemistries such as fluorocarbon based plasmas or$SiCl_4/Cl_2$ [19]. HBr/O_2 processes etch the silicon by formation of $SiBr_4$ volatile species. The $SiBr_x$ bi-products are also deposited over all exposed surfaces where they are oxidized by atomic oxygen. Thus, thick SiO_xBr_y passivation layers are deposited on the silicon sidewalls that will protect the gate sidewall during the subsequent TiN and HK etch steps.

Addition of metals into the gate stack implies an increased complexity in the development of suitable gate etch recipes. New process steps are required to obtain the desired final gate pattern. These new challenges will be further discussed in Chapter V but a brief description of HKMG etch process is presented.

After Silicon etching, an **N_2 flash** is carried out to further stabilize the silicon sidewall passivation and prepare TiN surface for etching. After polysilicon over etch, the polysilicon sidewalls are protected by a $Si_xO_yBr_z$ type passivation layer. In an N_2 plasma processing, this passivation layer reacts with Nitrogen that will contribute to the removal of halogen species and densify the layer into a SiON type layer. Besides, the etching ability of N_2 will remove remaining polymer residuals over TiN by formation of CN_x volatile products [23].

High-K Metal Gate (HKMG) etch consists in three steps; TiN main etch, TiN over etch and high-K etch step.

TiN main etch step is based in Cl_2/CH_4 plasma where Cl_2 is the main etchant forming $TiCl_x$ and NCl_x volatile compounds [25]and CH_4 may act as a deoxidizer of TiN surface by formation of CO volatile species. It can also help to the TiN etching process by forming volatile CN species or as a passivation agent forming amorphous carbon (a-C:H) deposition over TiN and silicon sidewalls [26].

TiN over etch is also carried out in Cl_2 based plasmas diluted in N_2 [27]. N_2 is used here to protect TiN sidewall and avoid lateral etching.

Finally, gate patterning is finished by a **high-k etch** step in BCl_3/Cl_2. Initially HfO_2 was etched in pure Cl_2 forming $HfCl_4$. However, this plasma condition leads to notched TiN profiles and silicon substrate recess. Thus, as already explained in Chapter I, BCl_3 gas was added to increase the selectivity towards the Silicon substrate. The B helps to break the Hf-O bonds and increases the HfO_2 etch rate by formation of BO and $HfCl_x$ volatile compounds. However, when the Boron meets the underneath silicon substrate, it forms B-Si bonds that help to initiate a BCl_x deposition and stop the silicon etch reaction. By this way, an infinite selectivity is obtained [28].

To characterize the gate etch process and the plasma/surface interactions, several material characterization techniques are used. The most important characterization techniques are summarized in the following section.

II.3 Characterization techniques

The characterization techniques used in this work can be separated into two main groups:

- The characterization techniques for the **physico-chemical analysis of material** modifications before and after plasma exposure. More particularly, to study the modifications of photoresist and SiARC materials, **FTIR, Raman, TGA, XPS, AFM and Ellipsometry** were used. For the analysis of the TiN modifications, **XRD** techniques were also used.
- The characterization techniques for **process qualification**, notably, SEM and TEM microcopies were used for morphological characterization, while CD-SEM and AFM were used for dimensional control.

A summary of all the characterization techniques with their intrinsic errors is shown in Table 1.

Table II-1 Summary of the statistical errors of all characterization techniques used in this work

Process Characterization		Material Characterization		CD and LWR Metrology	
Technique	**Error (units)**	**Technique**	**Error (units)**	**Technique**	**Error (units)**
Ellipsometry	± 2nm	XPS	± 5%	CD-SEM (GS)	± 1nm
SEM (Cross Section)	± 5nm	FTIR, Raman	± 4cm^{-1}	CD-SEM (CD)	± 0.4nm
TEM	< 1nm	XRD	± 0.01-0.02º	CD-SEM (LWR)	± 0.2nm
		TGA	± 10ºC	AFM	± 0.1nm

It should be considered, that the TEM and XRD techniques were carried out in collaboration with E. Latu-Romain and P. Gergaud expert engineers in each technique.

II.3.1 Material physic-chemical characterization techniques

The physico-chemical characterization was carried out over three different materials: Photoresists, SiARC and TiN. For the characterization of the Photoresist materials, FTIR, Raman, Ellipsometry, XPS, TGA and AFM techniques were used. For the SiARC materials, only Ellipsometry, XPS and AFM techniques were used. The TiN characterization was carried out using XRD and AFM techniques.

II.3.1.1 Ellipsometry

This is a non destructive technique for the optical characterization of a material within the whole volume and allows to determine the thickness and the optical indexes (n, k) of the deposited materials. It is based in the principle that, the polarized light changes its polarization when it is reflected over an interface [29]. In an etch process, this can be very useful because it allows to determine the etch rates of each material with different etch processes. For our experiments, the etch rates were measured either on full-sheet wafers using a S300-Ultra™ellipsometer fabricated by Rudolph Technologies, or over t-Box structures on patterned wafers using a SpectraFx 200™ ellipsometer fabricated by KLA-Tencor. Unless specified, all the etch rates shown in this work refer to etch rate measurements taken on full-sheet wafers.

II.3.1.2 Fourier Transform Infra Red Spectroscopy (FTIR)

a) Principle

The Fourier Transform Infra Red spectroscopy (FTIR) is an optical characterization technique that works in the infrared domain (λ=400-4000cm^{-1}). This technique is based on the interaction between the materials and the irradiation of an incident infrared beam. Thanks to this technique, it is possible to determine qualitatively and quantitatively the different chemical bonds composing the analyzed film [30].

This technique is based on the principle that, when the photon energy of the incident light beam is close to that of the vibration energy of a molecule, the molecules will absorb the incident irradiation that leads to a diminishing of the intensity of the transmitted light. Depending on the irradiation wavelength, the spectrometer geometry and the molecule mass distribution, the chemical bonds will present different vibration modes. These vibrations are gathered into two main families: the elongation modes and the deformation modes. The elongation modes (i.e. Stretching) correspond to an atomic movement along the bond axis (Fig II.10a &b), while the deformation modes (i.e. Bending) are vibration modes that deform the molecule and may occur in different directions as shown in Figure II.10(c to f).

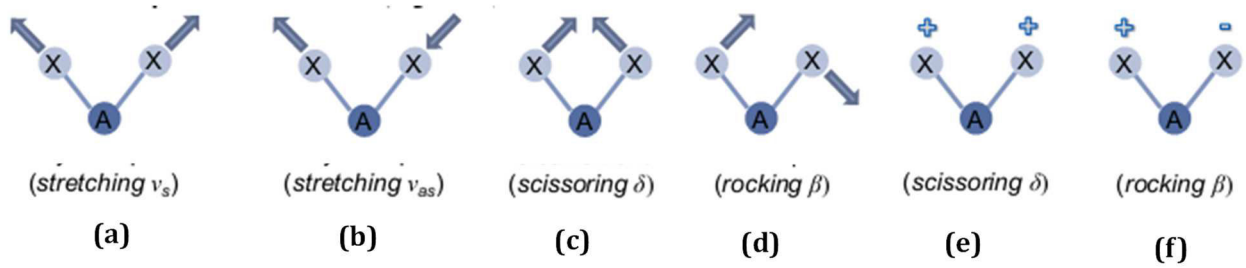

Figure II-10 Elongation and deformation vibration modes of an AX_2 molecule

The analysis of the absorption of all these characteristic vibration modes gives us an idea of the material volume composition.

b) Spectra acquisition methodology

In this work, the FTIR equipment used is a QS3300 infrared spectrometer from ACCENT society. The incident angle between the infrared beam and the analyzed substrate is 60º. A DTGS (i.e. Deuterated Triglyzinesufate) detector is used for transmitted light collection. The obtained FTIR spectra present a resolution of4cm^{-1}.

The spectra are obtained by averaging 150 successive measurements. The spectra acquisition is done in three steps. First, to remove the contributions of the equipment environment (air, CO_2 and H_2O contamination…) a FTIR spectrum of the background is taken and automatically removed from the analyzed sample spectra. However, usually some remaining peaks between 2320 and 2360cm-1 are observed, due to the CO_2 air composition variations from one measurement to another. Then, in a second measurement, the silicon substrate FTIR spectrum is recorded. Finally, the FTIR analysis of the deposited film on silicon is carried out. **By the subtraction of the silicon FTIR spectrum to the sample spectrum it is possible to obtain a clean spectrum of the deposited film without background or substrate contributions.** However, due to parasitic reflections that occur within the different interfaces in the analyzed sample, often, the resulting spectra present a non uniform baseline. **Correction of this baseline was performed by modeling the baseline with a linear curve that**

passes through the points at 4000, 2800, 1900, 1500, 1100, 700 and 400cm^{-1} considering that no absorption peaks are present at these positions for the analyzed samples. Afterwards, this curve is subtracted from the film spectra in order to obtain perfectly flatten FTIR spectra that can be compared between them. This technique is mainly used for photoresist characterization.

c) FTIR analysis of 193nm Photo-resists

FTIR is a very interesting technique for photoresist characterization because it provides some information concerning polymer chemical structure and its evolution during plasma etch processes. As an example the FTIR spectra of two different 193nm photoresist films ("Resist A" and "Resist B")used in this study are compared in Figure II.12. To better understand the FTIR spectra analysis, an example of a typical 193nm PR structure with its main functional groups is shown in Figure II. 11.

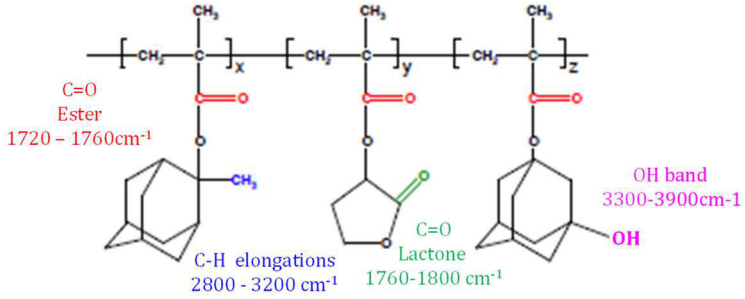

Figure II-11 Schematic representation of a 193nm photoresist

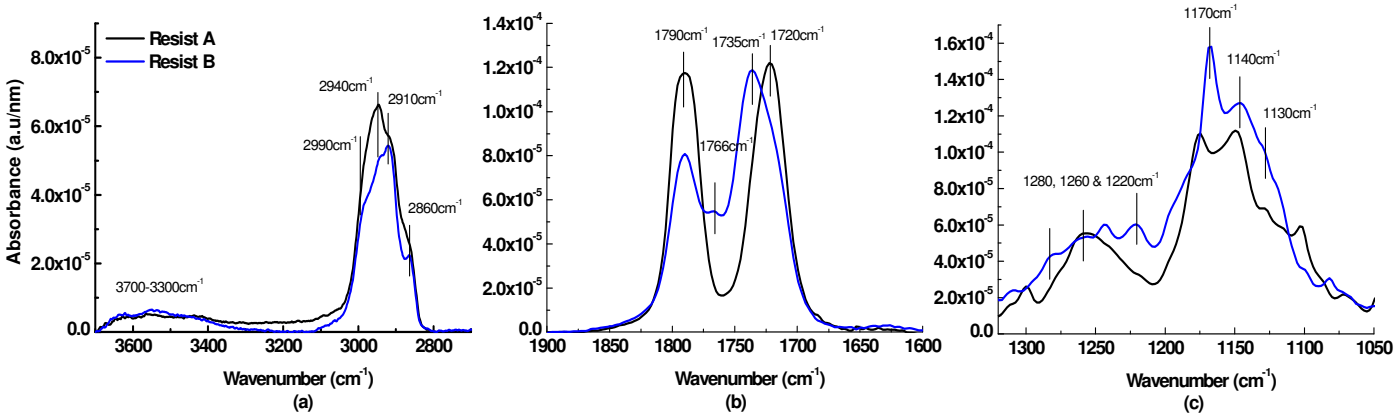

Figure II-12 (a) OH and CH stretching regions, (b) C=O stretching region and (c) COC stretching region of the FTIR spectra of two different 193nm photoresist after spin coating and PAB bake.

The FTIR spectra of the photoresists present three main characteristic regions:

Figure II.12 (b) shows the spectra range between 1900-1600cm^{-1} corresponding to the C=O bond stretching of lactone and ester groups. The peak at 1790cm^{-1}is typically attributed to lactone C=O stretching [11] [31] while the ester absorption peaks are typically seen around 1725-1705cm^{-1} [11] [31]. In our case, the peak at 1720cm^{-1} mainly present in "Resist A"is reported as an ester group that links the pendant groups to the main chain. In "Resist B" this peak is less intense, and the photoresist presents a major peak at 1735cm^{-1}, that certainly represents another Esther group within a different environment [32]. "Resist B" photoresist also shows presence of another absorption band at 1766cm^{-1} [33].That could be attributed to another lactone group with a different environment

The spectra between 3100-2800cm^{-1} corresponding to the C-H stretching modes are presented in Figure II. 12(a). "Resist A" and "Resist B" present slightly different C-H environment. The peak at 2990cm^{-1} is attributed to an alicyclic compound typically assumed to be the protective group [31]. The irresolute peaks at 2940cm^{-1} and 2860cm^{-1} are mainly attributed to CH_3 and CH_2 stretching absorptions respectively, coming from the main chain and the alkyl pendant groups [32].

The symmetric and asymmetric stretching absorptions of the different C-O-C groups linking the pendant groups to the main chain are shown in Figure II. 12 (c) and correspond to the absorption bands between1300-1050cm^{-1}. An increased aromatic ester (i.e. lactone) absorption is observed in "Resist B" (peaks at 1280cm^{-1}, 1260cm^{-1} and 1220cm^{-1}) [32] together with an increased presence of cyclic esters (1140-1130cm^{-1} absorption band) [32].

II.3.1.3 Raman Spectroscopy

The Raman technique is a non destructive optical technique that is based on the inelastic scattering of an incident wavelength by the analyzed material. The difference in energy between the incident photon and the Raman scattered photon is equal to the energy of a vibration of the scattering molecule. Raman scattering differs from infrared spectroscopy in that the former is concerned with the changes in the bond polarizability whereas the latter is concerned with the change of dipole moment. Thus, depending on the polymer symmetry, some vibrational modes can be optically active in Raman and not in FTIR. In particular, Raman brings additional data with respect to FTIR by providing detailed information on the symmetric bonds present in the polymer (such as C-C or C=C bonds) while the FTIR is more sensitive to high polarity bonds such as C=O (1700-1800 cm^{-1} region) and C-O-C (1100-1200 cm^{-1} region) stretching vibration modes. [34]

For our experiments, the Raman spectra are collected using a Jobin Yvon/Horiba LabRam spectrometer equipped with a liquid nitrogen cooled charge coupled device detector. **Experiments are conducted in the micro-Raman mode at room temperature in a backscattering geometry. The 632.8 nm line of He/Ne ion laser is focused to a spot size close to 2 μm using a x50 Olympus objective. Spectra from different experiments are calibrated using Si spectra at room temperature whose raman shift is at 520.7cm^{-1}.**

II.3.1.4 Thermo Gravimetrical Analysis (TGA)

The Thermo Gravimetric Analysis (TGA) is a thermal analysis that determines the thermal stability of a polymer by measuring its mass loss as a function of the temperature. This technique helps to determine a polymer's several characteristic temperatures, such as, the thermal deprotection temperature (T_d). In this work it has been most particularly used to determine the differences in the thermal stability of the two different photoresist platforms.

In this work, TGA 2950 equipment from TA Instruments is used, which consists in an oven and a high precision weighing scale. The equipment is kept within a controlled environment with a continuous nitrogen flow to avoid undesired reactions.

For the analysis, the photoresist materials need to be in a powder structure. Therefore, the PR films are first, scratched out from the silicon wafer using another silicon piece as a "razor". **To obtain a good resolution, a considerable polymer mass is required (1-2mg)**, which sometimes requires scratching out a whole 300mm photoresist wafer. This PR powder is then weighted in the TGA weighing scale as a

function of the temperature. **For our experiments the temperature ramp was set to 10ºC/min.** An example of a TGA thermogram is shown in Fig II. 13.

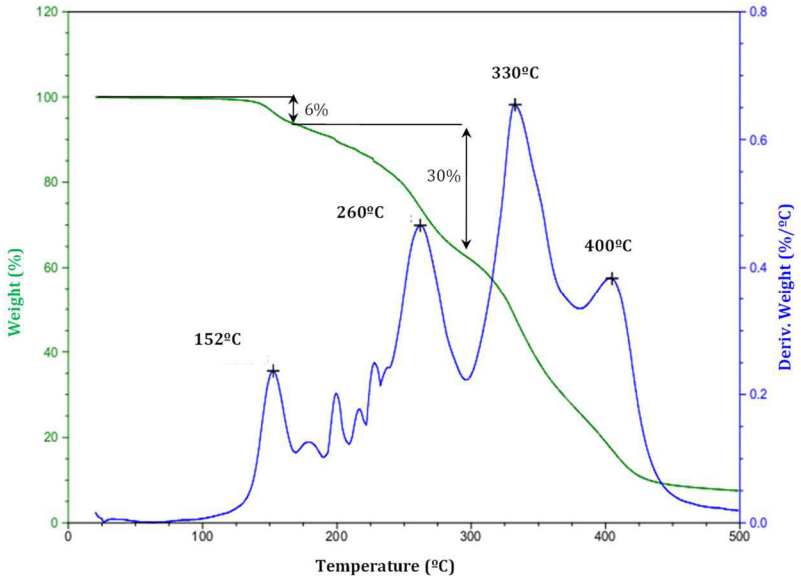

Figure II-13 TGA thermogram of the "Resist A" 193nm photoresist

An important mass loss at a given temperature is attributed to the outgassing of species from the photoresist, and a peak is observed in the derivate of the mass loss signal. The out-gassing temperature is typically attributed to the temperature at the peak maximum. Typically, the peaks at T<300°C are attributed to pendant group outgassing, while the peaks above 300°C are attributed to the polymer backbone degradation. The first peak, in our example at 152°C, is usually attributed to the *Thermal deprotection temperature (Td)*, the temperature at which the pendant groups are thermally activated and cleaved from the main chain. In the given example of Fig II.13, several peaks are observed within the 150ºC and 200ºC range, which correspond to a total mass loss of 36%. This can be attributed to the presence of many different pendant groups that are degraded at different activation temperatures. This example illustrates the complex analysis of photoresist materials.

It should be considered that this technique is carried out over powder materials, and their thermal behavior may be different from thin photoresist films.

II.3.1.5 Atomic Force Microscopy (AFM)

The Atomic Force Microcopy (AFM) is a microscopy technique that allows characterizing the topology variations of the analyzed surfaces. The principle is based on the scanning of a surface with an AFM probe that consists in a tip supported by a cantilever. Due to the interactions between the material surface and the AFM probe, we are able to determine the distance between both at each analyzed point and form an image [35].

In this work, to limit probe degradation and modification of the analyzed surface (i.e. for soft materials such as photoresists) **our experiments were carried out using an AFM "*Tapping mode*".** In this condition, the cantilever undergoes a forced oscillation at high frequencies (300 KHz). The amplitude of the oscillation is adjusted in order to have an intermittent contact between the sample surface and the AFM probe. The measurement of the oscillation amplitude and phase allows the reconstruction of the surface topography and the chemical composition of the surface with an atomic scale resolution.

In this work, we used an AFM enviroscope from Bruker Instruments with an Olympus AC160TS AFM probe. **For the image collection, the amplitude of the probe oscillation was set at 1V. 1x1µm AFM images were obtained where 512 measurement points are captured over 512 scan lines. The generated images are then treated using WSxM software.** This gives us the surface Root Mean Square (RMS) roughness of analyzed materials.

II.3.1.6 X-Ray Photoelectron Spectroscopy (XPS)

a) Principle

The X-ray Photoelectron Spectroscopy (XPS) is a non destructive technique that allows qualitative and quantitative analysis of a material surface composition (except from H and He atoms) over a several nanometer thickness (~9nm) [36]. Note that polymers are full of hydrogen atoms which will not be detected by this technique.

Its principle is based on the photoelectric effect. An X-ray with known *hv* energy will transmit all its energy to an electron in the core of an atom. In consequence, this electron is ejected from its orbital with a certain kinetic energy (E_k).

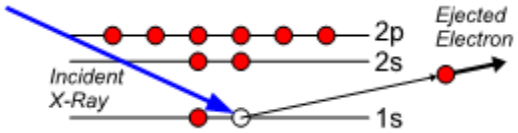

Figure II-14 Photoelectric effect principle

The emitted photoelectrons undergo inelastic collisions within the material and lose some part of their energy. Only some of them will have enough energy to reach the surface and be collected. Therefore, the analyzed depth is not dependent on the X-ray penetration depth (~10µm) but on the ability of electrons to reach the surface (~95% of the collected electrons come from the surface's first 10nm).

In the detector, the electrons are separated according to their kinetic energy. This kinetic energy of the photoelectron is representative of the binding energy of the electron to the atom core, and is defined by the following Equation [37]:

$$BE = hv - E_k - W_{spec} \qquad \text{(Eq.II.1)}$$

Where, *BE* is the binding energy, *hv* is the energy of the X-ray photon, $E_k$is the measured electron kinetic energy and W_{spec} is the working function of the detector.

Therefore, by measuring the kinetic energy of the ejected electrons from the analyzed surface, it is possible to determine their binding energy that depends on the analyzed element and its chemical environment.

The binding energy of a photoelectron is sensitive to the electro-negativity of its neighboring atoms. In other words, if we consider E_B the binding energy of a photoelectron coming from an A atom within an A-A matrix (reference solid matrix), the energy of this photoelectron will be sensibly different (E_B') if the A atom is linked to a different B atom (A-B bonds). The chemical shift between these two binding energies corresponds then to $\Delta E = E_B' - E_B$.

If the B atom is more electronegative than A, then ΔE>0 and the XPS peaks are shifted towards higher binding energies. In revenge, if B is less electronegative than A, then ΔE<0 and the XPS peaks are shifted towards lower binding energies. A schematic representation of the chemical shift principle is shown in Figure II. 15. The chemical shift effects of different B neighbors forming the environment of the A atom are independent and additive.

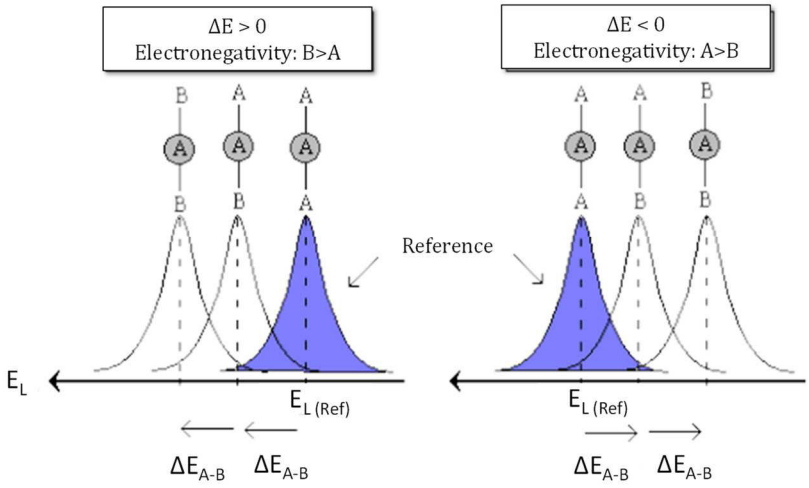

Figure II-15 Schematic representation of the chemical shift as a function of the electro-negativity of the B neighboring atom

It should be considered that measured chemical shift, ΔE, is always identical for all the electronic levels of an atom.

b) Experimental set up

All our experiments were carried out in a Tetha300 XPS fabricated by ThermoScientific™ in Figure II.16.

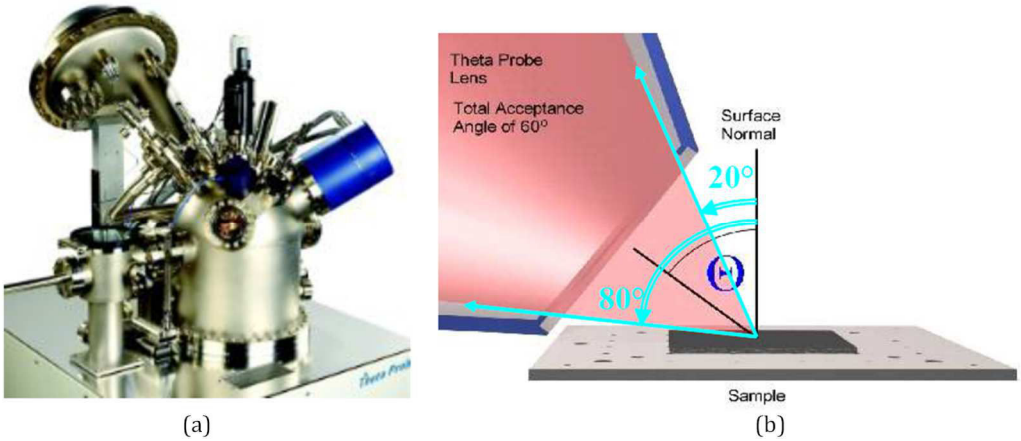

Figure II-16 (a) image of the Teta300 XPS and (b) sketch of the CCD detector principle

This equipment has been modified to connect it to an Applied Materials DPS etch reactor. This allows the analysis of material's surface composition after plasma exposure without contamination due to air exposure. However, since our processes were developed in a LAM Ex reactor, we could not benefit from this option. It should be considered that in our experiments the samples have been exposed to atmosphere conditions for a maximum of 5min.

The system is equipped with a high resolution X-ray aluminium monochromatic source. This is formed due to the energetic electron bombardment of an aluminum electrode that extract electrons from the aluminum atom's core. Relaxation of aluminum atoms leads to the emission of Al Kα X-ray photons at 1486 eV. The X-ray beam is then filtered by a monochromator and irradiated towards the sample. This results in a beam diameter of 20µm -100µm for sample surface scanning. The X ray beam interacts with the substrate material which will emit photoelectrons according to the photoelectric principle. The reflected photoelectrons are collected by the CCD detector which has an angle of acceptance of 60°. This allows collecting photo-electrons emitted from 20 to 80 ° compared to the normal at the surface. The photoelectrons are then directed towards a two dimensional detector (x , y) that can discriminate the photoelectrons depending on their energy (with 128 channels along the x axis) and depending on their collection angle (with 96 channels along the y axis). By this, the detector is capable to discriminate the photoelectrons depending on their collection angle (θ) which may vary between 23.75º (normal to the surface) and 76.25º (tangential to the surface). The scanned depth is dependent on the emission angle, and can be estimated by the following Equation:

$$d = 3\lambda\cos\theta \qquad \text{(Eq.II.2)}$$

Where d, is the analyzed thickness (nm), λ is the mean free path of the emitted photoelectron within the analyzed material (nm) and θ the photoelectron emission angle (degrees).

Therefore, by varying the photoelectron collection angle (i.e. measuring the flux of electrons as a function of the emission angle) the surface composition as a function of the scanned thickness can be determined. For example, the electrons measured at angles near ~76º are representative of the sample extreme surface composition (i.e. 1-2nm) while the electrons detected at ~23º come from deeper layers (i.e. 7-8nm) [36] [38].

The Theta300 system is also equipped with an electron flood gun that allows charge effect compensation for the XPS analysis of insulating thin films such as oxides or photoresists.

In this work, the Angle Resolved XPS (AR-XPS) technique was used to analyze the plasma impact on photoresist and SiARC materials exposed to the SiARC etch process (c.f. Chapter IV). **To ensure suitable resolution but reasonable analysis time, the photoelectron pass energy towards the analyzer was fixed to 100eV while the analysis step size is fixed to 0.1eV or 0.05eV (i.e. for Carbon compositions). To limit the number of scans, in all experiments the Dwell time was fixed to 200ms.**

c) Quantification method

To determine the concentration of each species, the peak integrals need to be calculated, and for this, Avantage Data System adapted software is used, which is able to fit the experimental data and determine the relative atomic composition of the sample surface. Due to the photoelectron inelastic collisions within the analyzed material, the XPS spectra present an important background that need to be removed in order to obtain a more precise estimation of the peak's surface area. Therefore, a linear baseline was used to delimit the spectra background. Then, spectral decomposition is carried out; which consists in determining within a complex spectrum, the elemental signal repartition, that represents the characteristic photoelectrons of an orbital, an atom or a chemical environment. In Figure II.17, for example, the spectrum is decomposed into four peaks that correspond to the signals of four different chemical environments (E_B, E_B', E_B'' and E_B'''). The peak fitting is the convolution of a Gaussian and Lorentzien.

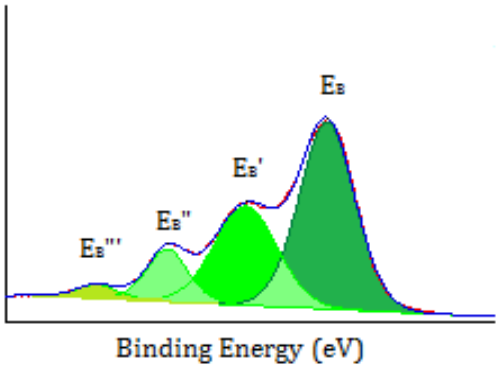

Figure II-17 Schematic representation of a peak with different chemical environments (E_B, E_B', E_B'' and E_B''')

The integrals of each peak's surface areas are proportional to the atomic concentration of characteristic elements within the scanned volume. For example, if we consider an A element, within a M material, the number of A atoms (n_a) within the M material can be calculated by the following formula:

$$n_A = \frac{I_A}{T_A S_A E_k^{0.6}} \qquad \text{(Eq.II.3)}$$

Where, I_A is the integral of the A peak surface, T_A is the transmission function of the analyzer, which is dependent on the electron kinetic energy, E_k is the kinetic energy of the photoelectrons, which depends on the Inelastic Mean Free Patch of electrons (IMPF) and the vacuum conditions and corresponds to $E_k^{0.6}$ in our setup conditions, and S_A is the Scofield coefficient of the A element. The Scofield coefficient accounts for the photoemission yield of the A atom, which is dependent on the electron kinetic energy. The photoemission yields for the main XPS peaks excited by an Al Kα beam were established by *Scofield et al* and are well reported in the literature [39].

Unfortunately, by XPS, we cannot directly determine the absolute concentrations of different species present in the analyzed surface. However, it is possible to determine relative concentrations of each element and thus determine the total surface composition as an atomic percentage. In that case, the relative concentration of the A element within the M matrix is represented as:

$$[A] = \frac{N_A}{\sum_i N_i} \qquad \text{(Eq.II.4)}$$

Where, ΣN_i is the addition of each element atomic percentage contribution. Using this method, the addition of all the relative contributions should be equal to 100%. However, it should be considered that the precision of this technique is assumed to be about 5%.

II.3.1.7 X-Ray Diffraction (XRD)

a) Principle

The X-Ray Diffraction (XRD) is a non destructive bulk characterization technique that offers qualitative and quantitative analysis of crystalline or semi-crystalline materials. This technique is typically used to examine the crystallinity and crystal structure of materials, and to determine the preferred orientation of crystal grains.

The technique is based on the fact that X-ray wavelengths are comparable to the inter-atomic distances within a material structure (i.e. several Å), and therefore the incident X-ray beams are scattered by

atoms in all directions. If atoms are randomly distributed (i.e. amorphous materials), scattered rays do not result in any destructive or constructive interaction. However, if atoms are arranged periodically in a crystal structure, the scattered beams present a phase relationship that leads to destructive or constructive interactions. Most of these interactions are destructive, which means that the resulting scattered beam intensity is equal to zero. However, in some directions the interfered beams are completely in phase and result in the formation of a diffracted beam (Figure II.18).

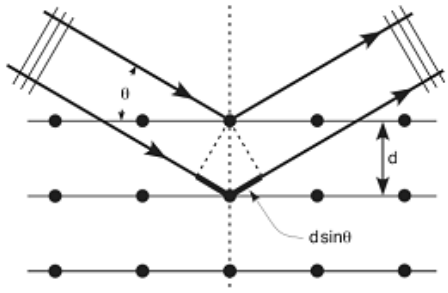

Figure II-18 Schematic representation of the diffraction principle

If crystal planes are the scattering surfaces, the relationship between the crystal structure and the diffracted beams is represented by the Braggs equation:

$$n\lambda = 2d\sin\theta \qquad \text{(Eq.II.5)}$$

Where, n represents the order of diffraction, λ, is the X-Ray irradiated wavelength, d, the spacing between atomic crystal planes and θ the scattering angle.

Therefore, the Bragg's law represents the minimum periodicity condition required for the X-ray beam to be diffracted by a set of parallel planes. The diffraction intensity, though, is not directly representative of the amount of diffracting crystals but is also dependent on the structure factor of the material to be analyzed. Basically, the structure factor is a mathematical description of the crystal scattering ability, which considers the relative phases of the scattered waves for a given scattering angle. The structure factors are different from one crystal structure to another and most of them can be found in reference database [40].

b) Experimental Set up: In plane XRD

The XRD analyses were carried out with a Smartlab system from Rigaku. Depending on the position of the incident X-ray beam and the detector, two different XRD analysis methods are defined: Out of plane XRD [41]and in-plane XRD [42].

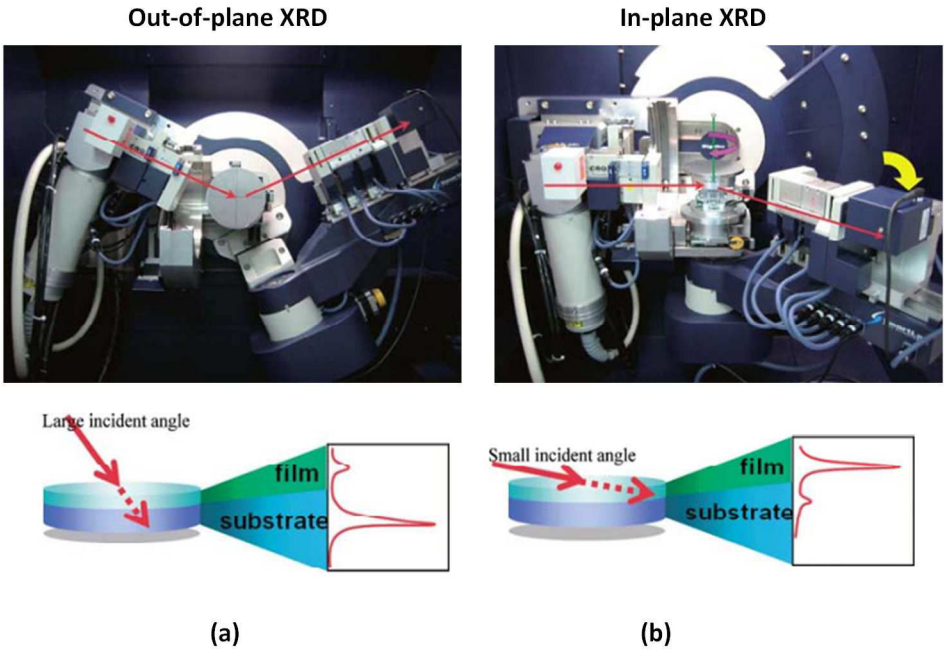

Figure II-19 Comparison of (a) Out-of plane XRD and (b) In-plane experimental set up and penetration depth

As it is shown in Figure II.19, in Out-of-plane method, the source and the detector are set with a given angle, θ, according to the analyzed surface (Figure II.19a). In other words, the incident beam is placed with a large angle towards the surface, and the resulting diffraction beam is pointed out from the sample surface. In this configuration, the X-rays will penetrate deep within the sample, which is interesting when thick films need to be studied. However, it is not suitable for thin-film XRD analysis because the sample signal will be lost within the background (i.e. substrate signal).

In an in-plane XRD method, both the source and the detector are placed tangent to the analyzed surface (Figure II.19b), and therefore, the resulting diffraction beam lies parallel to the sample's surface. In this configuration, the sample surface is irradiated by a grazing X-ray beam that travels long distance within the thin film but without an significant penetration. This increases the signal of the thin film as compared to the substrate and allows XRD characterization without the disturbing contribution of the substrate background signal [42].

Both techniques give structural information of the analyzed material (Crystal orientation, grain size, texture…); however they do not look at the same lattice planes (Figure II. 20)

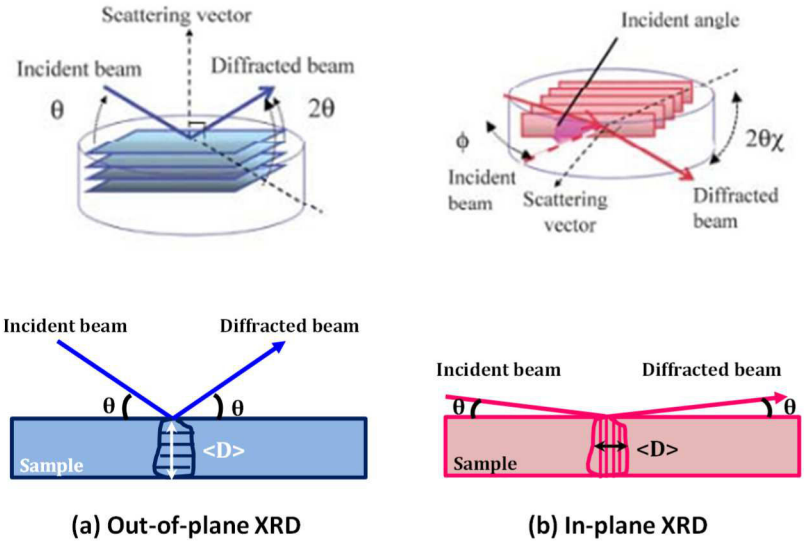

Figure II-20 Analyzed lattice plane orientation in an (a) out-of-plane XRD and (b) In-plane XRD techniques.

In an Out-of-plane XRD technique, the analyzed lattice planes are parallel to the sample's surface, while in an In-plane XRD technique, the measured lattice planes are normal to the sample's surface. This means that, with both conditions, the extracted information is not exactly the same. For example, if the crystal grain size want to be measured (<D>), each XRD technique will not give the same grain dimensions. In an out of plane XRD technique, the crystal's vertical size is measured (Fig II.20a). For example, if we consider a PVD deposited TiN film, whose crystal grains grow in a columnar fashion, the vertical grain size is typically similar or equal to the deposited film thickness. In revenge, the in-plane XRD technique measures the horizontal grain size (Fig II.20b) which can be modified by the deposition conditions.

In this PhD work, the XRD technique was used to characterize the microstructure of 10nm thick TiN films, and therefore, it seems clear that the In-plane XRD method is required. Besides, the characterization of the horizontal grain size of the TiN films is of a great interest because it can influence the gate CD variations and therefore, modifies the LER and the electrical performance of HKMG stacks. This information can only be obtained by using the In-plane XRD technique. **Therefore, for our experimental conditions, the In-plane XRD method was chosen. All the XRD experiments were done in collaboration with C. Suarez.**

c) TiN film XRD diffractogram analysis

An XRD diffractogram is unique and representative of a specific material composition. In fact, from the analysis of an XRD diffractogram, several structural information can be obtained, such as, the film composition, the crystal orientation and the crystal grain size. In our experimental conditions, the XRD spectra are collected over Polysilicon (24nm)/ TiN (10nm)/ HfO_2 (10nm) gate stacks (Figure II.21).

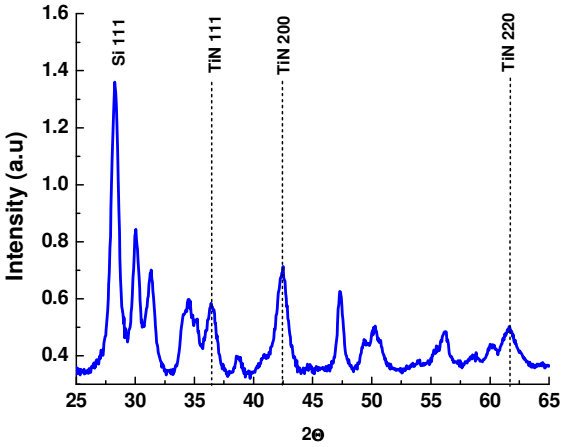

Figure II-21 XRD spectrum collected over a Polysilicon (24nm) / TiN (10nm) /HfO_2 (10nm) gate stack

In such a configuration, the XRD spectra are quite complicated because of the contribution of Polysilicon and crystalline HfO_2 peaks. For a better comparison, spectra were normalized by the Si [111] peak intensity at 2θ = 28.24° [40]and only the TiN peak contributions are discussed.

To determine the composition of the deposited films, the peak 2θ position is analyzed. Each peak position depends on the primitive cell dimensions of the crystal structure and is therefore representative of the film composition and crystal orientation. In the given example, it can be observed that the TiN used for the HKMG depositions is composed of δ-TiN phases with three main crystal orientations; [111] orientation at 2θ=36.46° [8] [4] [43], [200] orientation at 2θ=42.38° [43] and [220] orientation at 2θ=61.48° [43].The XRD equipment has a 2θ position precision of 0.01-0.02 and therefore slight variations in the peak positions may indicate modifications in the TiN lattice. For example, if contaminant (i.e. Oxygen) are dissolved within the TiN film in an interstitial position, they may slightly expand the TiN lattice which results in a slight shift of the 2θ position towards lower values. The dimensions of the lattice can easily be determined using the Bragg equation.

To determine the preferential orientation of the TiN crystals, the ratios between the integrals of each TiN contribution need to be calculated. For example, for the 10nm TiN film shown in Figure II.21, since three crystal orientations are observed, the [111]/[200], the [111]/[220] and the [200]/[220] ratios can be compared (Figure II.22).

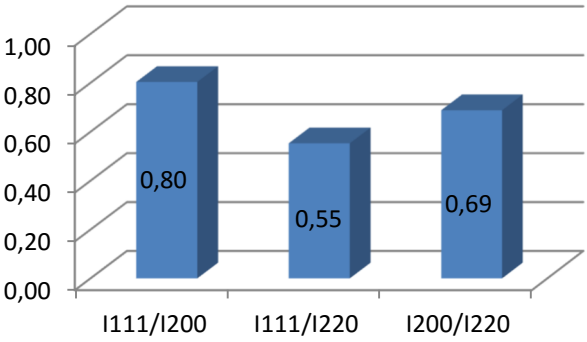

Figure II-22 Calculation of the [111]/[200], the [111]/[220] and the [200]/[220] peak integral ratios

In this case, the deposited thickness has a preferential orientation of 220>200>111. Note that we are working with an In-plane XRD technique and therefore, the measured orientation does not correspond to the TiN surface, but the TiN sidewalls.

Finally, to determine the crystal grain size, the sharpness of the XRD peak is analyzed. Thus, sharp XRD diffractograms indicate the formation of densely and uniformly packed crystalline structures. In revenge, broad and not defined XRD peaks are representative of weakly crystallized or nearly amorphous film structures. For grain size metrology, the experimental data is fitted using adapted software and the peak surface is used for grain size determination following the Scherrer method [44]:

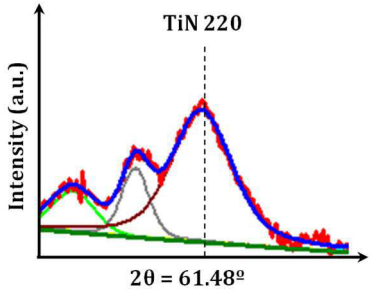

Figure II-23 Representation of the fit of a TiN 220 peak at 2θ = 61.48°

$$< D >= K\lambda/[\beta cos(2\theta/2)] \qquad \text{(Eq.II.6)}$$

Where, *<D>* is the grain size (nm) *K (K=1)* is an instrumental constant, λ is the incident monochromatic beam wavelength (~0.15nm), β is the peak width in Radian (i.e. the peak surface divided by the peak intensity) and 2θ (radian) is the Bragg angle at the peak maximum position.

Thanks to the XRD diffractrogram analysis a good characterization of the TiN film microstructure can be carried out.

II.3.2 Process Qualification techniques

For the process qualification, TEM and SEM microscopy techniques were used for the morphological characterization of our gate patterns, while CD-SEM and Tilted AFM techniques were used for CD control and LWR metrology.

II.3.2.1 Scanning Electron Microscopy (SEM)

In this technique, the sample is scanned by an electron beam. The retro-diffused and secondary electrons are then collected selectively by a detector that transmits the information to a screen that converts the signal into an image. Depending on the sample topology or the analyzed material more or less electrons are retro-diffused which allows us to detect a change in the sample morphology (by the secondary electrons) or composition (by retro-diffused electrons) [45].

In this work, a High Resolution SEM 5000 from Hitachi was used for cross section morphological analysis of gate patterns. To improve the resolution the detector is cooled with a liquid nitrogen flow. This equipment was mainly used for lithography stack (PR/SiARC/SoC) profile characterization and therefore **only the secondary electrons were collected (SE mode).To avoid excessive photoresist degradation under the electron beam, images were taken with an acceleration voltage of 3kV and an emission current of 10nA.**

II.3.2.2 Transmission Electron Microscopy (TEM)

The TEM allows us to measure the dimensions of the gate profile obtained after etch with a sub nanometer scale resolution. For this analysis, first a thin lamella is extracted from the sample using a focalized ion beam set in a FIB-STEM Helios NanoLab™ platform fabricated by FEI. Then the sample is analyzed using a TecnaiOsiris™ High-Resolution TEM (HRTEM) from FEI. In this technique, an electron beam is focalized normal to the silicon substrate. Afterwards, by the help of magnetic lenses, the electrons transmitted or diffracted by the sample are then focalized in the plane of the image. By this, high resolution images can be obtained [46].

II.3.2.3 CD-SEM Metrology

a) Principle and Experimental Set up

The CD-SEM is a top view Scanning Electron Microscopy (SEM) technique that allows the metrology of the gate CD and Roughness (LER, LWR). The interest of this technique is that it allows measuring a large number of gate patterns in a short amount of time.

In this technique, the sample is scanned by an electron beam. The produced secondary electrons are then collected selectively by a detector that transmits the information to a screen that converts the signal into an image. Each (x and y) point scanned by the SEM is given by a gray level that corresponds to the number of secondary electrons detected by the SEM at this position. Depending on the sample topology or the analyzed material more or less secondary electrons are emitted which allows us detecting a change in the sample morphology or composition.

In this work, the SEM-CD 4001 from Hitachi was used for top-view CD and roughness metrology. The working tension of the system can be fixed between 300V and 800V with a low current of 6pA to 10pA which allows the formation of an electron beam with a diameter close from a nanometer. By this, different structure CDs can be measured with a maximum resolution of 0.4nm. This equipment is able to measure over 200mm or 300mm wafers without sample cleaving and at relatively high speeds (~100measurements/15min). Therefore it is one of the most used metrology techniques in the microelectronic industry.

b) Image acquisition

In order to obtain a good quality CD-SEM images, adapted image acquisition parameters need to be chosen. For this, it should be considered that certain materials, such as photoresists, are very sensitive to the impact of electron beams and undergo shrinkage phenomena when exposed to intense electron doses [47]. Therefore, the image acquisition parameters need to be optimized in order to obtain a reduced photoresist degradation but a good image contrast so that the metrology algorithms work efficiently. For this, different acquisition parameters can be modified:

- The acceleration tension (300V, 500V, 800V)
- The Integration time (i.e. number of frames, from 4 to 256 frames available)
- The number of pixels per image (512, 1024, 2048px)
- The scan size (Square or Rectangular)

The acceleration tension varies between 300V, 500V and 800V and determines the electron beam size and energy. When strong acceleration tensions are applied, smaller electron beams can be obtained for image scanning. This improves the image resolution, but results in energetic electron beams that

strongly degrade fragile materials, such as photoresist. Therefore, the acceleration tension of the scanning electron beam is adapted depending on the nature of the analyzed materials.

The integration time (i.e. higher number of *frames*) determines the electron dose received by each pixel composing the image. To improve the signal/noise ratio, the electron dose should be increased. And this can be obtained by working at higher number of frames (from 4 to 256 frames available in our CD-SEM equipment) [48]. However, it should be considered that, increasing the number of frames implies increasing the exposition time and therefore the material damage.

The number of pixels composing the image can also impact the image acquisition. In fact, for an image generation, the image's X and Y dimensions are divided by the number of pixels in X and Y direction, respectively. Thus, the image is defined by a pixel grid that is scanned by the electron beam to carry out the acquisition. Consequently, a higher number of pixels within an X or a Y direction, results in a smaller pixel size and an improved resolution. Therefore, depending on the resolution required, the number of pixels can be adjusted between 512px, 1024px and 2048px.

The resolution can be different along the X and Y directions, and this is obtained by modifying the scan size. In our equipment, two different scan sizes are available: a square scan and a rectangular scan. In a square scan mode, the same resolution is obtained along the x and y axis. In revenge, a rectangular scan mode allows working with different magnifications along the x and y axis. This is particularly important for precise roughness metrology where significant line lengths need to be scanned (2.8µm) with good resolutions.

In all our experiments the CD and LWR are measured over 20 images with dense line patterns comprising at least five gate lines per image.

For Photoresist line metrology, a 300V tension and 16 frames are used to avoid material degradation under exposure of energetic electron beams [47].
For silicon gate patterns, since no pattern deformation occurs under electron irradiation, the applied tension is increased to 800V and the number of frames is increased to 32 frames in order to obtain better signal to noise ratio. In both cases, the working current is always fixed to 10pA.

The CD metrology is carried out over 512x512 pixel images using a square scan mode. By this method, the CD is measured over relatively short gate lengths (~1.4µm)but it is enough to calculate an averaged gate CD value.
For the roughness metrology, 1024x1024 pixel images are captured using a rectangular scan mode with a 300K magnification along the x axis while and a 49K magnification along the y axis. This results in pixels of 0.45nm and 2.75nm along the x and y axis, respectively, which allows obtaining a good resolution along the x axis and a maximum observation field along the y axis.

c) Image offline analysis

The obtained images are then analyzed offline using Terminal PC software from Hitachi. This consists in the application of an algorithm that analyses the image contrast variations and determines the right and left line edge positions. For this, typically a threshold measurement method is used for edge detection. In our experiments a threshold of 80% was used which assumes that at the line edge the pixels present an 80% of the maximal signal.

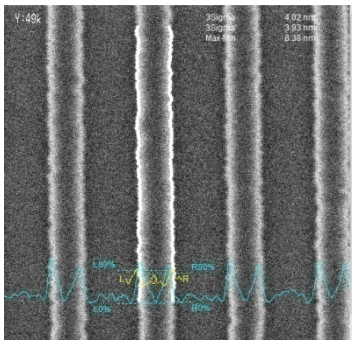

Figure II-24 CD-SEM image of a PR pattern. The position of the measurement points is shown for the middle line.

To carry out the measure, a measurement box is defined that determines the zone to be measured. This box is defined considering the following parameters:

The Inspect Area (IA) that represents the amount of pixels along the Y axis that will be analyzed. In other words, it defines the measurement box size along the Y axis. The Inspect area should be then the biggest as possible in order to scan sufficiently long line lengths. In our process conditions (i.e. 1024x1024 pixels for LWR metrology) the box maximum size is fixed to 846 pixels, which corresponds to a maximum line length of 2.2µm. Long enough to ensure proper roughness metrology.

The *measurement point (MP)*, which corresponds to the number of measures (N) carried out within this box (i.e. the number of CD measured along the Y axis). The maximum authorized in the Terminal PC software is 400.

The Sum Line (S), or the amount of averaged pixels along the Y direction. The sum-line allows improving the signal/noise ratio, however, if too many measurement points are averaged (i.e. high sum lines), the short distance information is reduced.

The *Smoothening* is the number of pixels that are averaged along the x direction. An increase in the smoothening allows improving the signal/noise ratio.

A schematic representation of all these factors is shown in Figure II. 25.

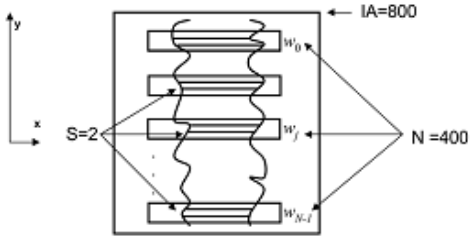

Figure II-25 Schematic representation of the Inspect Area (IA), Measurement point (N) and Sum Line (S) parameters

All these parameters must respect the following relation to obtain a suitable sampling:

$$IA = N \times S \qquad \text{(Eq.II.7)}$$

If this relation is not respected, and IA>NxS, the sampling is considered as insufficient. If IA<NxS, then, the sampling would be excessive.

For CD metrology, the main important parameters are the threshold, to ensure proper edge detection. However, for the LWR metrology, the longest line length possible needs to be scanned, in order to obtain enough information about all the roughness frequencies. The maximum Inspect Area authorized by the Terminal PC software is 80% of the image size, which corresponds to an IA of 800 pixels in 1024x1024 pixel images. In the same manner, for a latter data treatment (i.a. for suitable PSD analysis of the LWR) a maximum number of measurement points is also required.

Therefore, for all our processes, the CD and LWR metrology is carried out using 400 measurement points with a sum-line of 2 which, according to the IA=NxS relationship defines a measurement box with an Inspect Area of 800 pixels. Finally, the Smoothing along the X axis was fixed to 25 pixels because, according to the previous studies [49], it allows to limit the image noise without impacting the roughness. By this, the CD and roughness is measured over gate lines of 2.152µm.

d) LWR metrology protocol: The noise extraction method

In a general manner, every metrology equipment gives a measure with a certain noise component. In CD-SEM metrology, the images present an important measurement noise due to errors during the electronic signal treatment. Therefore, the measured roughness results therefore from the combination of two components, the "*real Roughness*" and the "*noise*" that can be considered as random noise [50]

$$\sigma^2_{measured} = \sigma^2_{real} + \sigma^2_{noise} \qquad \text{(Eq.II.8)}$$

In our case, a precise roughness metrology needs to be obtained, and therefore, this noise component needs to be removed from the measured value. For this, we could, for example, increase the number of frames in order to increase the signal/noise ratio. However, as already explained, when soft materials are measured, such as photoresists, this strategy can be damaging for the analyzed structures.

Therefore, a Matlab software was developed in our laboratory by *Azarnouche et al* to evaluate and extract the noise component from the roughness measurement and thus, obtain the real gate roughness [50].

More precisely, this method consists in calculating an experimental Power Spectral Density (PSD), that is equivalent to the square of the Fourier transform of the CDs measured along a line pattern within a CD-SEM image, and then, adjust the experimental data with an analytical function.

A PSD is the representation of a signal's power as a function of the measured frequencies. Concerning the LWR, this can be imagined as the CD deformations with a large spatial period (low frequency roughness) and the deformations with a smaller spatial period (high frequency roughness). It is therefore important to measure the LWR over long line lengths in order to account of the low frequency deformations.

To obtain a smooth PSD that can be adjusted correctly, 50-100 line measurements are required. For each line, a PSD is calculated and the experimental PSD will be the average of the whole 50-100 individual PSDs (Figure II. 26). The integral of the PSD curve is equal to σ^2_{meas}, and is therefore representative of the line width roughness (LWR = 3σ).

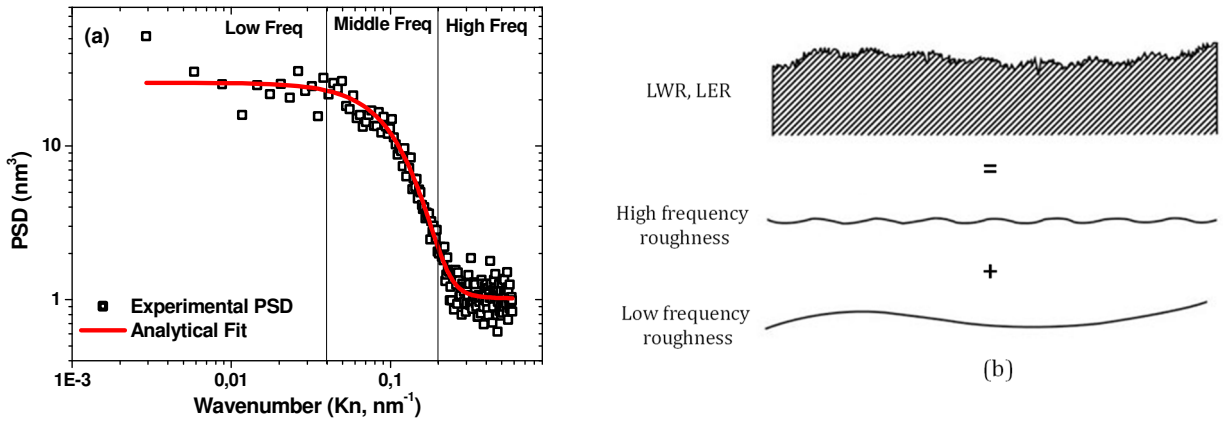

Figure II-26(a) Power Spectral Density (PSD) representation of the line width roughness and (b) a schematic representation of the low frequency and high frequency roughness over a line edge.

In the discrete case where the line length (L) and the measured interval have finite values, the discrete PSD (P_n) is defined as follows:

$$P_n = \frac{L}{2\pi}\langle |F_n|^2 \rangle_{N^*} \qquad \text{(Eq.II.9)}$$

Where, N^* is the number of samples, L is the line length, and F_n is the discrete Fourier transform. This PSD can be also written as a function of the auto-correlation function (ACF) as follows:

$$P_n = \frac{\Delta_y}{2\pi N}\left[\sum_{m=0}^{N-1} 2R_m \cos\left(k_n m \Delta_y\right)(N-m)\right] \qquad \text{(Eq.II.10)}$$

Where, N is the number of measurment points within the box (MP = 400), Δ_y is the measure interval determined by $\Delta_y = L/N$ (where L is the line length, therefore, $\Delta_y$corresponds to the sumline which is in our case twice the size of the pixel along y), k_n is the wavelength (where, kn = $2\pi L$ x n, with n = (0, 1, …, N-1)), m is the difference between two points (j , l), and finally, R_m is the autocorrelation function (ACF).

Azarnouche et al proposed working with an ACF that corresponds to a self-affine fractal function. The fractals are typically used to describe the irregularities of a given structure. If we consider the roughness as an irregularity of a given surface, we can define it by a fractal model. In our case, the given

surface is considered as a self-affine surface, which means that if the observation window is modified, the observed structure does not have the same appearance. The self-affine fractal function describes the roughness by three different terms; σ, or the roughness amplitude, α, the roughness exponent (i.e. gives an indication of the surface irregularities of the line edge, if α is small, the line edge is very irregular) and ξ, the correlation length (i.e. the length over which we can consider that two points within a line edge are independent). Thus, the auto-correlation function of a self-affine surface is given by:

$$R_m = \sigma_{real}^2 e^{-\left|\frac{m\Delta_y}{\xi}\right|^{2\alpha}} \quad \text{(Eq.II.11)}$$

In order to account of the measurement noise, the ACF function can be rewritten as follows:

$$R_m = \sigma_{real}^2 e^{-\left|\frac{m\Delta_y}{\xi}\right|^{2\alpha}} + \sigma_{noise}^2 \delta_m \quad \text{(Eq.II.12)}$$

Where δm is the Kronecker signe. By this, the auto-correlation function is defined by two components, the first, representing the real roughness variance (σ^2_{real}) and the second, which represents the noise variance (σ^2_{noise}).

Thus, if we combine Eq.II.12 and Eq.II.10 we obtain the P_n function shown in Eq.II.13 which will be used for the analytical fitting of the experimental PSD data.

$$P_n = \frac{\Delta_y}{2\pi N}\sigma_{real}^2\left[\sum_{m=0}^{N-1} 2e^{-\left|\frac{m\Delta_y}{\xi}\right|^{2\alpha}} \cos\left(k_n m\Delta_y\right)(N-m)\right] + \frac{\Delta_y}{2\pi}\sigma_{noise}^2 \quad \text{(Eq.II.13)}$$

Thanks to the analytical adjustment method, the measurement noise is determined and subtracted from the experimental PSD. Afterwards, the surface integral of the experimental PSD (without noise) is calculated, which will therefore correspond to the real roughness variance (σ^2_{real}). By this method we can therefore obtain a real LWR value that is not biased by the measurement noise.
However, for PSD representation, logarithmic axes are used, which do not allow working with negative values. If the experimental PSD are plotted without any measurement noise, the curve will be deformed within the high frequency zone. To avoid representation issues, an arbitrary white noise of 1nm is added to the data.

For further information concerning the noise extraction method, the lector can refer to Laurent Azarnouche's PhD work [50].

So in conclusion, the CD-SEM is a very useful technique for CD and LWR metrology that allows measuring a large number of measurement points over any type of structures in a short time. However, it still presents some limitations. Firstly, concerning the latest CMOS technologies, the CD-SEM resolution becomes an issue for the CD metrology of 20nm gate lines. Besides, it can impact fragile materials such as photoresists and result in resist shrinkage and CD deformations. And finally, it remains a top view metrology technique that gives no information over the buried layers in complicated gate stacks.

To get rid of these limitations, and more particularly, for this PhD to be able to measure the buried TiN sidewall roughness a novel metrology technique that was developed in our laboratory has been used: The Tilted AFM metrology.

II.3.2.4 Tilted AFM Metrology

To analyze the sidewalls of a sample by AFM metrology, two different strategies can be used. Either we tilt the AFM probe, or the sample itself.

In the LTM laboratory, *Fouchier et al* have designed a variable angle sample holder that allows measuring the sidewall LER of gate lines on a tilted sample [51]. The angle position (θ) can be varied between 0º (i.e. horizontal sample) and 90º (i.e. vertical sample) (Figure II. 27a). The tilt angle is chosen in order to scan the full pattern height including the bottom. Depending on the sample dimensions, the tilted angle needs to be optimized in order to obtain an accurate measurement.

The influence of the tilt angle variations has already been reported by *Fouchier et al.* [51]. According to their analysis, at high tilt angles, lower LER values are measured at the bottom of the pattern probably because the tip hardly reaches the feature bottom. In revenge, if too low tilt angles are used, probe sticking effects are more probable which can also influence the LER estimation. Working with tilt angles in a 45º-55º range does not seem to have a strong impact on the LER determination and the averaged LER values obtained present an error of ±0.2nm, which is close from the standards for the AFM techniques (0.1nm).

The used AFM probe is an Olympus AC160TS AFM probe that has a curvature radius of 7nm and is placed at the very end of the cantilever, to be able to measure the bottom of 3D features. The scan direction is parallel to the feature length. However, to measure accurate sidewall LER over a scanned line without being bothered by the neighboring line, specific network dimensions are required. As shown in Figure II. 27b, the space between lines, needs to be at least twice the height of the scanned pattern. If this condition is not respected, some parts of the sidewall may not be imaged due to shadowing effect or because the tip may hit the top of the neighboring pattern.

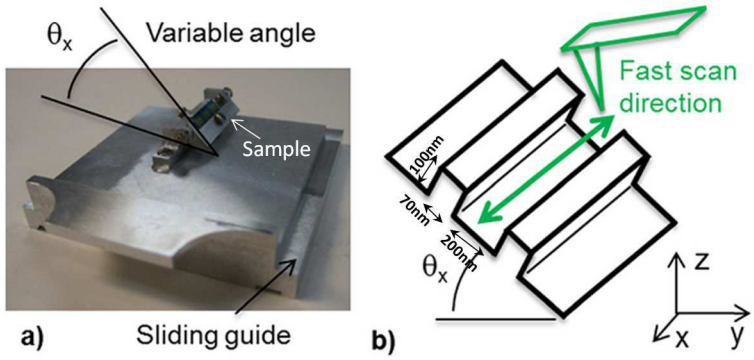

Figure II-27 Experimental set up: (a) variable angle sample holder and (b) Scan direction with respect to the features. For suitable AFM metrology the space between patterns need to be at least twice the pattern height.

For the image collection, the AFM analysis was carried out using a Tapping mode with an amplitude set point at 1V. The measurements were carried out with a holder tilt angle that may vary from 45º to 55º. 2x1µm AFM images were obtained where the LER metrology was carried out over a 2µm gate length within line network of 1µm composed of 9 gate patterns. For each image 1024 measurement points are captured over 1024 scan lines. The generated images are then treated using WSxM software.

However, since the images are collected on tilted samples, the captured images are therefore also rotated along the x axis. Besides, due to the imperfection of the sample holder position, the capture

images may also present a certain deviation angle along the y and z axis. Therefore, to ensure accurate LER metrology and gate profile determination, a Matlab software has been created to rotate the image to the horizontal. This data treatment is followed by an interpolation of the rotated data points on a grid. This allows a better organization of the data points by using well defined step sizes along the x and z axis to simplify the LER calculation. Finally, the LER of the analyzed feature is calculated at each z height positions of the interpolation grid. The same process is carried out with the 9 patterns composing the AFM image.

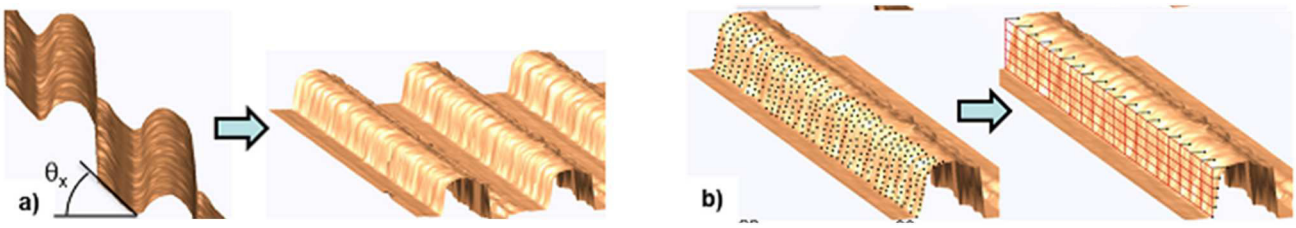

Figure II-28 AFM data processing: (a) Image Rotation and (b) Interpolation

This technique allows measuring the LER for the whole scanned pattern height. Besides, the averaged half profiles along the feature length can also be calculated. For a more statistical analysis, 2-3 AFM images are taken for each sample. The LER and pattern profiles are then calculated for the 9 patterns present within each image. The presented LER and gate profiles are the average of all pattern contributions.

It should be also noted that by AFM the measurement noise is very small (~0.2nm) and therefore, there is no need for a specific protocol for noise extraction and the obtained LER value can be considered as the real LER.

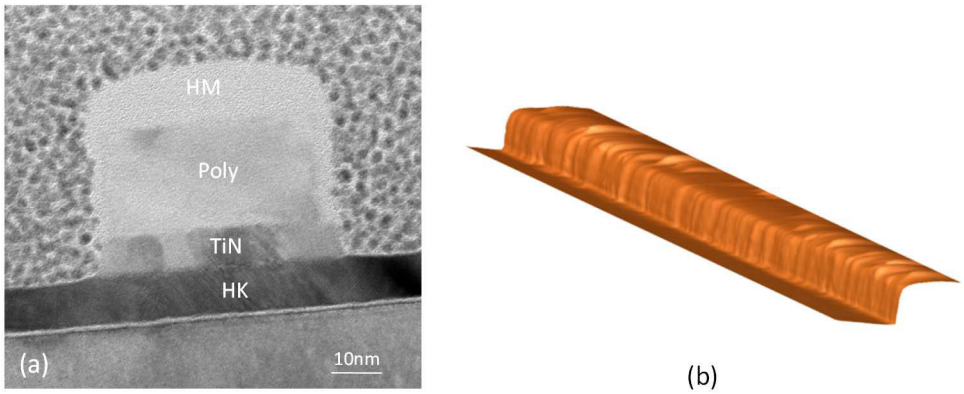

Figure II-29 (a) TEM and (b) Tilted AFM images obtained over the full gate stack after full etch

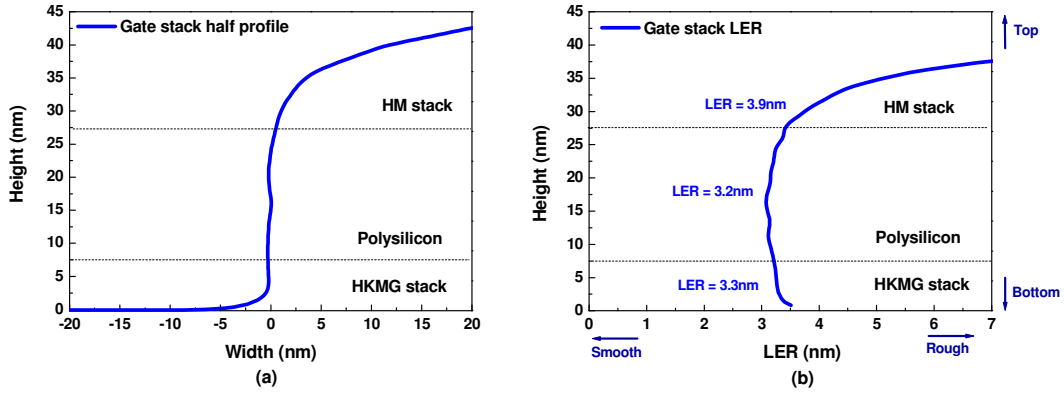

Figure II-30(a) Half gate profile and (b) LER evolution over the scanned pattern height for a full gate

As an example, FigureII.30 shows the half gate profile and LER evolution over the scanned pattern height for a full gate stack. For further comparison, images of the gate stack obtained by TEM and Tilted AFM are also shown in Figure II.29.

In Figure II.30a, the gate half profile evolution is shown. The interface between the HM, polysilicon and HKMG layers is determined according to other microscopy techniques, such as SEM or TEM. It should be considered that, since only one pattern sidewall is analyzed, only half profiles are obtained and no CD or LWR information can be determined. This technique allows the identification of profile variations such as notch, or tapered profiles.

In FigureII.30b, the LER is represented in the x axis while the pattern height is represented in the y axis. Averaged LER values are given for each material. In this case, the HKMG LER is the averaged LER value measured in the first ~7nanometers along the z axis. The polysilicon LER, is obtained by averaging the LER values measured between ~7nm and ~27nm along the z axis, and the HM LER is averaged within the last ~12nm. However, presence of flat surfaces at pattern bottom and also profile rounding at the pattern top sidewall lead to an increased error in the AFM metrology. Therefore, the first and last ~3nm are not considered for the calculation of the averaged LER values.

II.3.2.5 Comparison of CD-SEM and Tilted AFM LER metrology

The CD-SEM and AFM techniques are two complementary metrology techniques but, both present some advantages and disadvantages.

It should be considered that, the CD-SEM metrology is a statistical metrology, which allows measuring a large number of structures in a short time and gives CD and roughness information. With this technique, all the roughness components can be calculated (LWR, LER, ξ and α), a roughness spectral analysis can be carried out (i.e. PSD) and the correlation factors between both pattern edges can be estimated. Besides this technique is an in-line metrology technique that allows measuring any pattern within a 200mm or 300mm wafer. However, working with CD-SEM implies using energetic electron beams that may damage the fragile materials such as photoresists. Besides, this metrology remains a top-view technique and is compromised for a precise study of the LER and the roughness transfer mechanism in multilayer gate stacks.

On the other side, the AFM technique is long, not statistic and requires specific sample preparation (i.e. small samples with specific line networks). In addition, though the PSD analysis is also possible with

AFM techniques, this requires collecting a big amount of measurements which results in really long measure times, which cannot be considered in an industrial environment. Besides, only one pattern sidewall is analyzed and therefore, only LER information and half-pattern profiles can be obtained. However, it allows scanning the LER variations all along the pattern height in all type of gate profiles with complicated multilayer stacks. The averaged LER values of each layer contributions can be easily determined and gives us an information about the LER of buried layers such as HKMG stacks.

Tableau II-1 Advantages and Disadvantages of Tilted AFM and CD-SEM techniques

	Advantages	Disadvantages
CD-SEM	• Statistic • Allows spectral analysis • Online Metrology	• Top view metrology • Average LER estimation over the whole pattern height • Destructive on fragile materials (i.e. PR) • Resolution issues for sub-20nm features
Tilted AFM	• Improved Resolution • All the pattern height is analyzed	• Time consuming • LER analysis only • Sample cleavage required • Not possible to analyze dense line patterns

In conclusion, both techniques present their advantages and limitations but they remain complementary. Therefore, for the following studies, the CD-SEM metrology will be used to provide preliminary LWR and LER information, a spectral roughness analysis and to account of the correlation degree between both line edges. For precise roughness analysis, AFM metrology will be preferred. By this technique, the roughness transfer mechanism can be studied avoiding the uncertainties of the CD-SEM metrology.

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Chapter III. Gate shifting phenomenon on 14FDSOI Gate etch processes

As explained in Chapter I, in a transistor manufacturing process, gate patterning is one of the hardest stages to control. Along with downscaling, the specifications for a transistor manufacturing have tightened up to the nanometer scale. The major issue is the control of two main variability sources: Critical Dimension uniformity (CDU) and the Line Width Roughness (LWR) which are both limited to 10% and 12% of the targeted CD respectively, which corresponds respectively to 2nm and 2.4nm (for 20nm gate designs) as defined by the ITRS [1].

Besides, the presence of dense random 2D patterns in the integration of gate designs makes this task even more challenging.

To improve lithography performances, post-lithography treatments such as plasma treatments have so far been introduced to increase photo-resist stability and to improve LWR and CDU before pattern transfer [2].If such a strategy allows meeting the CDU and LWR requirements of the 32 nm technological node, it is not any more efficient to address the specifications of the latest CMOS technologies.

In this chapter, we describe a new patterning challenge induced by the addition of photoresist pre-treatments in 14FDSOI technologies, referred as Gate Shifting. In a first section, we discuss the mechanisms responsible for the gate shifting during cure treatments. Based on this understanding, we propose, in a second section, other cure plasma conditions to limit the gate shifting phenomenon. In this section, we also discuss the impact of those new cure conditions on both LWR and pattern transfer, and the compromise that has to be done.

III.1 Gate Shifting Issue

III.1.1 The Gate shifting phenomenon

For logic CMOS devices, contact to gate patterning has the tightest patterning specifications. The presence of dense random patterns in the integration of gate designs and the difficulty to etch small contacts between the gates makes this combination the most challenging one. **It has been found that during the gate etch process there is an intra-field pattern deviation where 2D gate patterns are displaced from their original position. The misalignment problems between transistor gates and contact holes may lead to gate to contact shorts that can reduce transistor electrical performance of a 50%.**

Figure III.1 presents planar description (Fig III.1 a, b, c) and TEM cross sections (Fig III.1 d) of two gates next to each other showing a strong local variation of contact to gate distance. By design there is no reason for these two transistors (G1 and G2) to be different as shown in FigureIII.1b. However, such pattern deformations are enough to compromise transistor electrical performance by increasing the probability to obtain gate to contact shorts.

The so called gate shifting is also visible on Figures III.1 (a, c) and is considered as a local pattern misalignment quite difficult to detect. In the planar description of the gate profile, rounded shapes caused during the patterning process are deviated from the original design (Figure III.1b). Pattern rounding is already known in lithography processes. Many studies have been done to correct pattern deformation by proper Optical Proximity Correction (OPC) modeling and design rules modifications regarding contact to gate placement [3] [4]. Anyway, despite the in-line corrections, this distortion remains noticeable suggesting a local gate deviation generated during patterning process and non-correctable at lithography level.

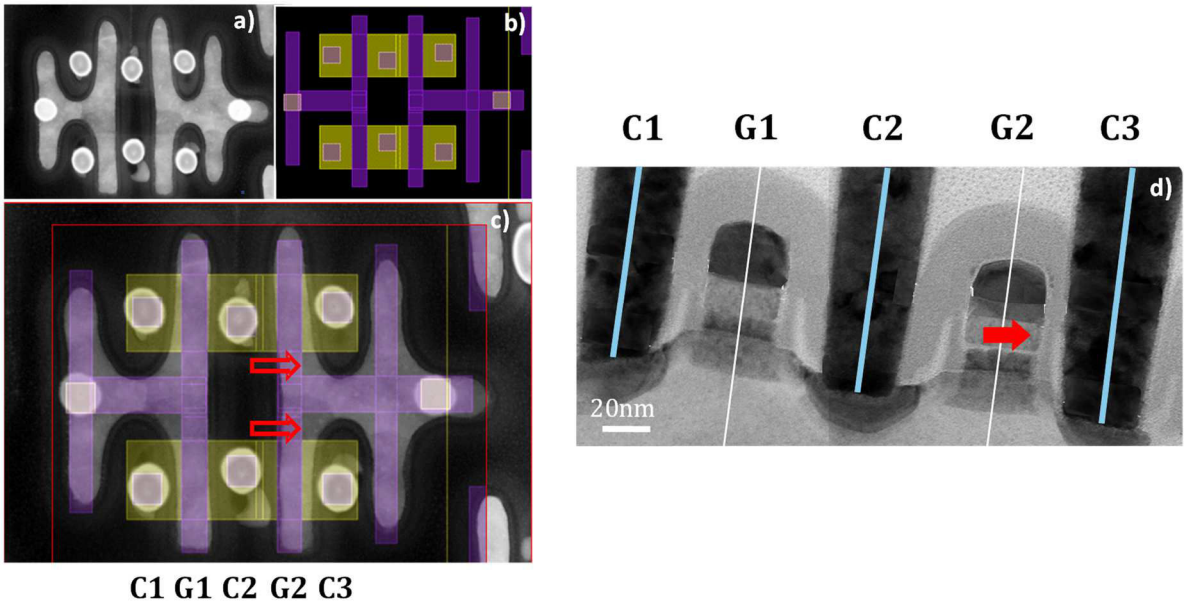

Figure III-1 Representation of localized overlay distortion: (a) Planar description versus (b) design is overlapped in figure (c) to show local overlay distortion (d)TEM imaging of two gates next to each other over the same wafer. The transistor on the right is shifted towards the right contact line. To help the lector, labels are added: C1, C2 and C3 represent the contact position, and G1 and G2 the gate line position.

This phenomenon, referred as Gate Shifting (GS) constitutes a new challenge for advanced gate patterning. The aim of this chapter is to study the mechanisms responsible of this gate misplacement and propose new strategies for proper gate patterning.

III.1.2 Origin of gate shifting

To better understand the origin of the gate shifting phenomena, the gate patterning process was closely studied. Figure III.2 shows CD-SEM images taken after lithography and etch steps. By closely comparing both steps we clearly observe that **the gate etch process has introduced some pattern deformations that lead to the gate shifting phenomenon.** Lithography pattern lines remain straight (Figure III.2a) while they are drifted from their original position (Figure III.2b) after full etch. Note that differences in pattern shape between both figures are due to CUT patterning and will not be discussed (refer to Chapter I for further details).

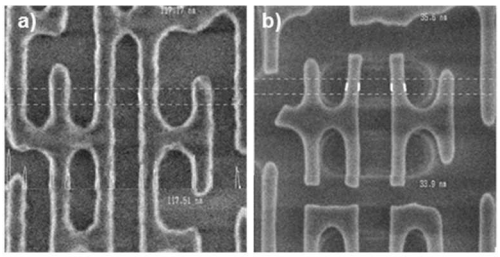

Figure III-2 CD-SEM images of a) photoresist gate patterns after lithography and b) after full etch

In order to determine which step within the gate etch process is the main contributor for the gate shifting, the gate etch process has been studied until the silicon patterning step (c.f. Chapter II, section II.2.2.3 for process details).

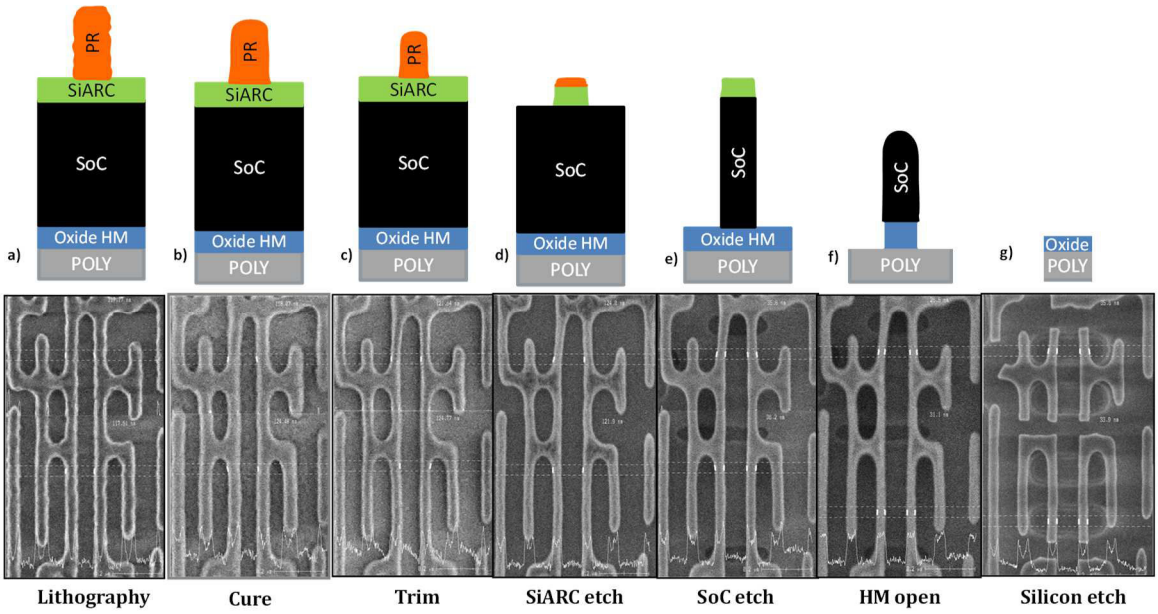

Figure III-3 Schematic representation and CD-SEM images of a gate pattern after a) lithography b) resist cure c) resist trim d) Si-ARC open e) SOC open f) hard mask open and g) silicon etch.

Figure III.3 shows top view CD-SEM images of gate pattern evolution during the whole gate etch process. Looking closely at each etch step, cure step seems to be the root cause of this phenomenon (Figure III.3b). It can be noticed that the photoresist pattern is modified compared to that after

lithography (Figure III.3a). Patterns are wider, with rounded shapes, compromising the pattern definition and the spacing between the features. When such deformations are observed in simple line patterns, they can easily be corrected by trim steps. Unfortunately, 2D pattern modifications cannot be corrected similarly. This can be seen in Figure III 3c where deformations observed after cure remain after trim. These deformations are then transferred into the rest of the gate stack without further modifications (Figures III.3d-g).

Since pattern deformations are caused during cure step, a possible solution to avoid the gate shifting phenomenon could be cure step removal. Top view images of 2D gate patterns with and without cure are shown in Figures III.4 (b&c) after exposure to SiARC etch steps.

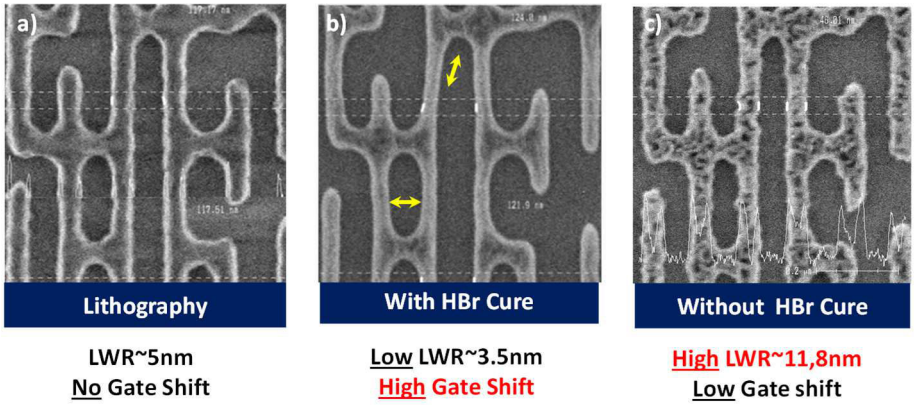

Figure III-4 Top view CD-SEM images of 2D gate patterns after (a) lithography and SiARC etch process (b&c), In (b) photoresist patterns have been exposed to HBr cure prior to SiARC etching. In (c) PR patterns are exposed to SiARC etch chemistries without cure. LWR values were measured by CD-SEM. Arrows are added to guide readers eyes and better illustrate pattern deformation.

Cure step removal leads to straight patterns with no deformation and no gate shifting (Figure III. 4c) compared to those previously exposed to HBr cure (Figure III. 4b). However, cure step removal results in severe LWR degradation after SiARC etch process.

A compromise needs to be found to limit the pattern deformation while preserving suitable pattern LWR. The mechanisms leading to gate shifting during the cure step need then to be clarified.

III.2 Mechanisms responsible for gate shifting during cure step

III.2.1 Impact of HBr cure step on photoresist patterns

Figure III.5 shows SEM cross-section images of photoresist patterns (referred later in the text as "resist B" used for 14FDSOI technologies) before and after HBr cure plasma process. It is clearly observed that photoresist patterns exposed to HBr cure plasma present a reflowed profile with an increased CD of 20% (Figure III.5 b). This behavior is totally different from what has previously been observed on old generation 193 nm photoresist [2] [5]. In previous studies [2] [5], it was observed that the resist pattern tends to shrink laterally and vertically and remain square when exposed to HBr cured plasma. The shrink was attributed to the outgassing of photolysis products followed by densification. On the other side, it was also demonstrated that if the resist pattern was only exposed to the VUV irradiation emitted by HBr plasma, the resist profile was rounded like reflowed. It was suggested that the dense carbon layer that forms on photoresist surfaces exposed to HBr cure prevents from resist flowing and maintain square profile (cf. Chapter I, section I.4.3.1)

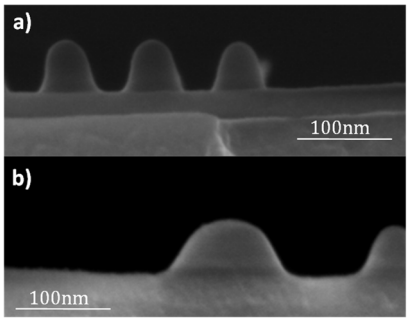

Figure III-5 SEM cross-section images of resist (referred later as resist B) pattern after a) lithography and b) HBr cure

This preliminary observation suggests that contrary to old generation 193nm photoresist, the 193nm photoresist used in this work and selected for the 14nm node at STMicroelectronics reflows during HBr cure process.

To better understand the mechanisms driving the photoresist reflow phenomenon two 193nm photoresist were compared: the first, is mainly used in C028 CMOS technologies (referred as "Resist A") and the latter is the polymer chosen for the latest 14FDSOI technologies ("Resist B"). Due to confidentiality issues, further information of both resists cannot be revealed.

Figure III. 6 compares the CD-SEM images of both photoresist patterns after lithography (a & c) and after HBr cure step (b&d).

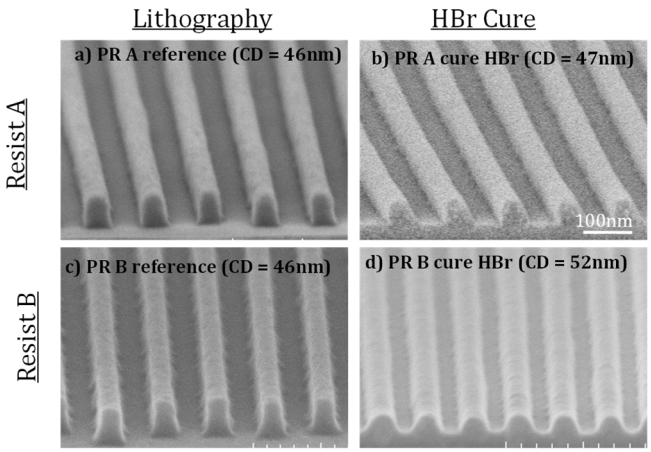

Figure III-6CD-SEM images of "Resist A" and "Resist B" photoresist patterns (a, c) after lithography and (b, d) after HBr cure

As shown in Figure III.6, "Resist B" line patterns swell and reach CD values of around 52nm after an HBr cure process. A more limited swelling is observed for "Resist A" where line CD increased only to 47nm. A graph representation of this CD increase is shown in Figure III.7.

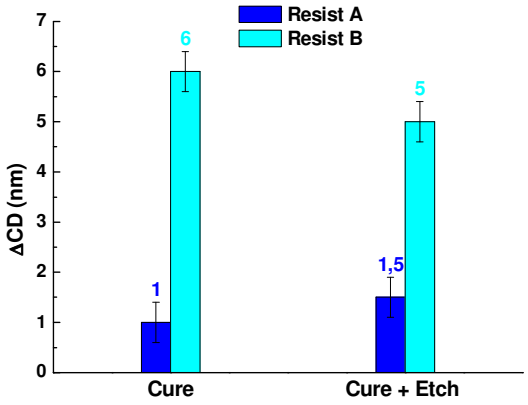

Figure III-7CD variation obtained by CD-SEM of patterns after cure and etch steps for both resists under investigation.

For "Resist A" photoresist, resist flowing is limited (~1nm) compared to that of "Resist B" (~6nm). This increased CD is then transferred into SiARC without further modifications for both photoresists.

Those preliminary results indicate that the flowing behavior is very dependent on the polymer nature.

FTIR analyses have been carried out on resists A and B to determine the chemical modifications induced by HBr cure plasma as shown in Figure III.8.

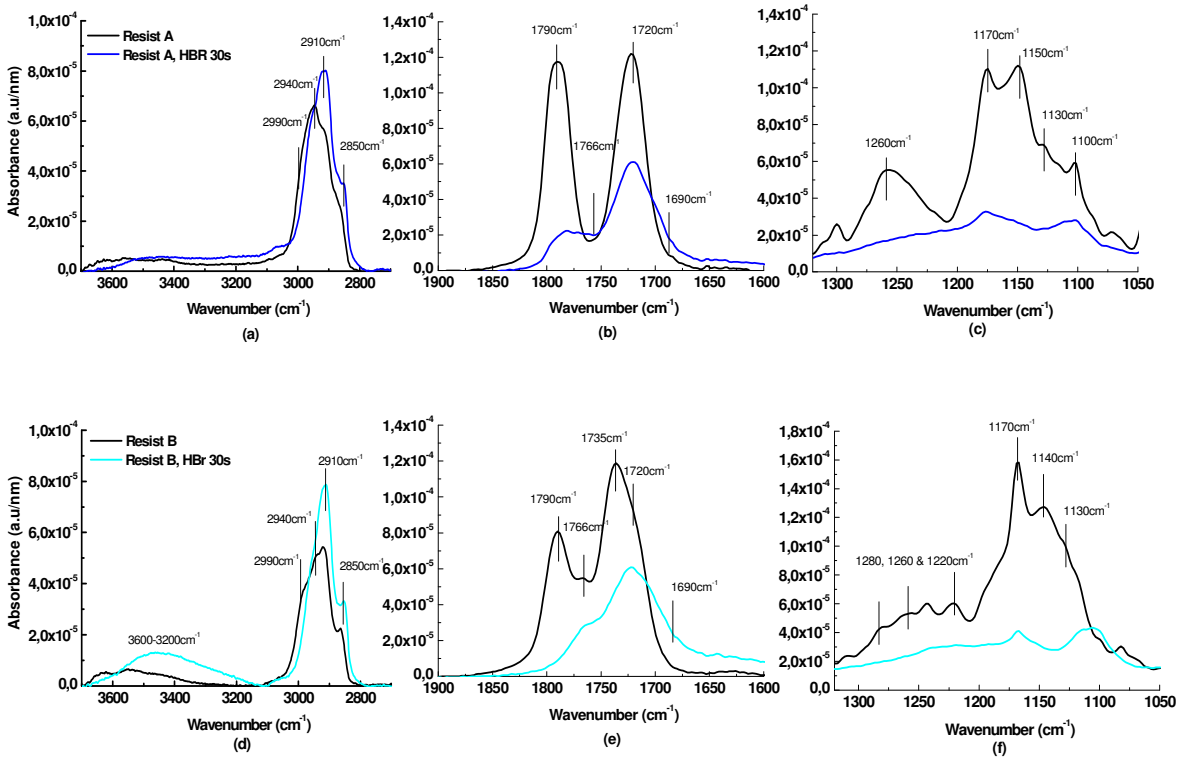

Figure III-8(a&d) OH and CH stretching regions, (b&e) C=O stretching region and (c&f) COC stretching region of the FTIR spectra of "Resist A" and "Resist B" photoresist after spin coating & bake and exposed an HBr cure plasma condition.

According to photoresist pristine FTIR spectra (Figure III.8 (a to f)) both resists present similar chemical structure after spin coating and bake (c.f. Chapter II) and it is equivalent to that of previous 193nm photoresists already reported in the literature [6] [7] [8]. The PR structure presents stretching modes corresponding to lactones (1760-1790cm^{-1}) and esters (1720-1760cm^{-1}) which are linked to the polymer's main chain by different C-O-C groups (absorption bands at 1300-1050cm^{-1}). Note that, "Resist B" has a complicated chemical structure with more than 6 different monomers therefore additional absorption peaks are also observed. The chemical modifications of both resists induced by HBr plasma are very similar to what has already been observed. HBr VUV irradiation induces lactone opening (decrease of C=O peak at 1790cm^{-1} and 166cm^{-1}, Fig III.8 (b&e)) and esters photolysis (C=O peak at 1720cm^{-1} and 1735cm^{-1}, Fig III.8 (b&e)) by the cleavage of the C-O-C bonds (irresolute peaks in Fig III. 8 (c&f)) that link ester groups to the polymer backbone. These lactone and ester groups are then removed from the photoresist film by forming CO and CO_2 [9]. In other cases, mostly for "Resist B", they may also remain in the film by formation of carboxylic acids (C=O peak around 1690cm^{-1}, Fig III. 8 (b&e), and OH band around 3600-3100cm^{-1}, Fig III.8 (a&d)). Following the same mechanism, scission of pendant groups (2990cm^{-1} peak in Fig III.8 (a&d)) and esters (peak at 1720cm^{-1}, Fig III. 8 (b&e)) occurs. The pendant groups are thought to remain within photoresist film and act as plasticizers [9] [10]. An increase of C-H bonds (2910cm^{-1} and 2850cm^{-1} peaks in Fig III.8 (a&d)) is also observed which may be due to the recombination of polymer fragments within the film or VUV induced polymer densification [11] [12].

Those analyses reveal that the HBr cure process has a similar impact on both photoresist, which is also identical to what was already observed on previous studies, and thus cannot explain why the "Resist B" tends to reflow more than "Resist A". It should be noted that the only difference between the two resists is the more significant amount of carboxylic acid in resist B (1690cm^{-1} and OH 3200-3600 cm^{-1} in Fig. III. 8 (d&e)). The small shift on the OH band position (from 3600cm^{-1} to 3450cm^{-1}) suggests the formation of carboxylic acids with a different chemical environment or can be attributed to the adsorption of water (H_2O) on the polymer matrix [8].

Another aspect that has been looked at is the presence or not of a carbon hard layer on the resist surface exposed to HBr cure [7]. To verify this, Raman analyses have been carried out after HBr plasma exposure on both resists A and B (Figure III.9).

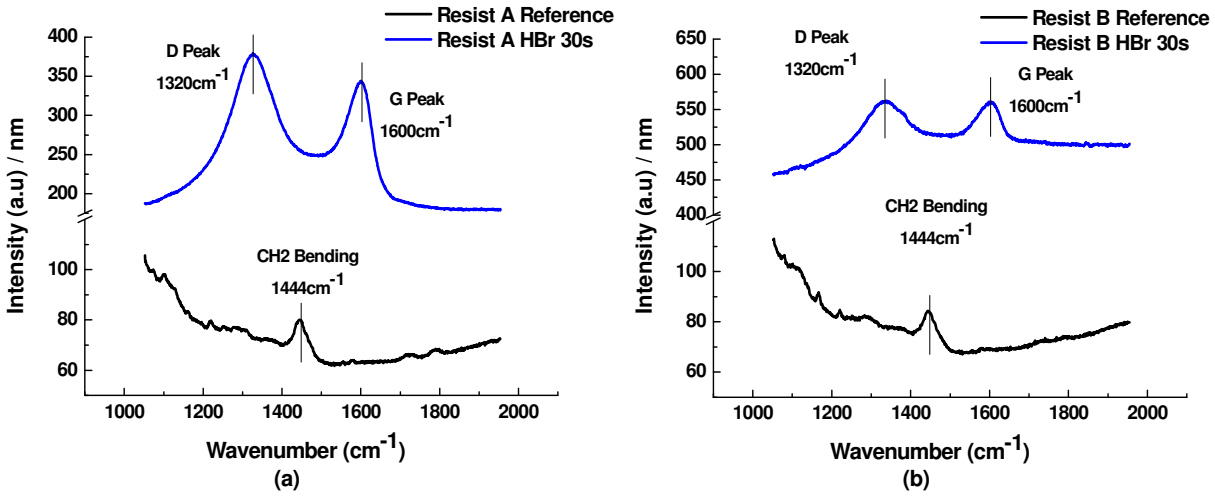

Figure III-9 Raman spectra of (a) Resist A and (b) Resist B before and after exposure to an HBr plasma during 30s

The Raman spectra of both reference photoresists is quite similar and only shows the presence of CH_2 bending modes at 1444cm^{-1}. After exposure to HBr plasma, the Raman spectra shows the presence of two new peaks at 1320cm^{-1} and 1600cm^{-1} referred as D and G peaks that reveal the presence of an amorphous carbon like layer on the resists exposed to HBr plasma [7] The G peak reflects the E2g zone center of crystalline sp^2-bonded graphite while the D peak is associated with disordered graphite [13]. The CH_2 bending modes at 1440cm^{-1} are probably present but they lie in the D region and therefore we neglect them for our analysis. This suggests that as for old generation 193nm photoresist, there is also the formation of a dense amorphous like carbon layer on both resists A and B.

These results show that HBr cure plasma leads to similar chemical modifications (ester and lactone decomposition within the resist bulk and formation of an amorphous carbon layer on the surface), whatever the chemical structure of the 193nm photoresist. However, it does not result in the same pattern profile and the same reflow.

Thus the main contributors for the resist flowing mechanisms need to be studied. The next sections review the main parameters influencing the resist flowing mechanisms.

III.2.2 Resist flowing mechanism

The resist flowing phenomenon is well reported in the literature. IBM proposed many patents in the application of photoresist reflow for tapered contact etching [14] [15]. Other groups, use resist flowing for residue encapsulation [16]or passivation [17]. Besides, from its applications in semiconductor industry, resist flowing has also been considered as a defectivity issue and is the target of many lithography publications [18] [19] [20] [21] [22]. In our case, the resist flowing is considered as a variability source that could lead to a performance loss as high as 50% depending on the products and the process conditions. Thus, this section is dedicated to better understanding the mechanisms that drive this resist flowing.

A fluid flow or “creep” is a consequence of the surface tension changes that will bring an energetically stable system towards a non-equilibrium situation. To recover the equilibrium, the system will deform, and this deformation, in our case, occurs by resist flowing.

The surface tension is a result of the intermolecular interactions. However, macroscopically, we can define it as the force acting at the interface when placing two different environments in contact together.

If we imagine a fluid, all molecules within the bulk are equally attracted towards neighbor molecules in all directions resulting in a null force within the fluid bulk. However, surface molecules are not fully surrounded by fluid molecules but also by air molecules. Due to the differences between liquid-liquid and liquid-gas interactions, the surface molecules present a resulting force different from zero. This resulting force is known as surface tension and thermodynamically is defined as the energy per unit surface area:

$$\gamma = dG/dA \qquad \text{(Eq. III.1)}$$

Where, γ is the surface tension, dG is the system energy and dA is the surface area, usually expressed in J/m^2

When three different environments are in contact, for example, a solid, a liquid and a gas, surface tension forces will be generated at each of the three interfaces, solid-liquid (SL), liquid-gas (LG) and solid-gas (SG) (Figure III.10a). Due to the presence of these three surface tensions, the system finds an equilibrium point where all the forces in the system are balanced (Figure III.10b).

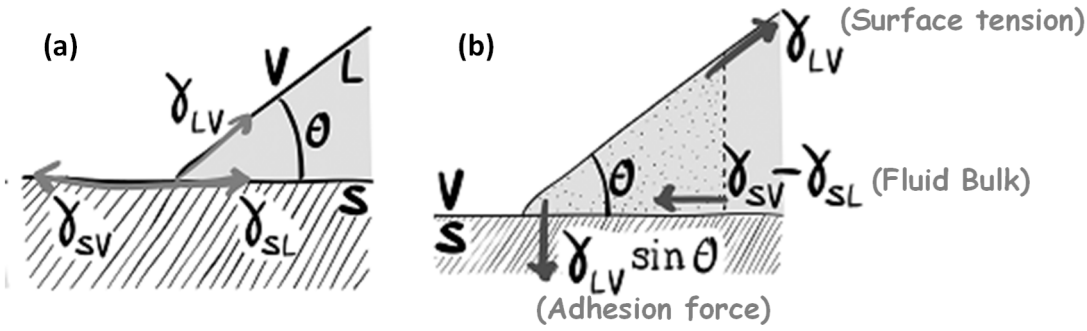

Figure III-10(a) Schematic representation of a Solid-Liquid-Gas system with the three surface tensions acting on a contact line balanced (b) Solid and liquid forces acting near the contact line. The three forces exerting on the system are the surface tension (γ_{LV}), the adhesion force ($\gamma_{LV}\sin\theta$) and the fluid bulk ($\gamma_{SV} - \gamma_{SL}$).Extracted from [23]

Since, for our applications, we want to define a resist flowing, we could consider the resist as a fluid at the interface with a solid surface (i.e SiARC) and a gaseous environment (i.e Air). Therefore, if we imagine a photoresist pattern, the three interfaces in equilibrium define the pattern shape; in other words, the surface tension will make the resist sidewall to be in equilibrium with no reflow.

However, the surface tension acting on each interface changes with the nature of materials forming the interface. Therefore, we could imagine that if one of our materials (PR, SiARC) follows a considerable change on its chemical nature or material properties, the surface tensions concerning this material may change.

Now, let's consider an external stress source, for example, photoresist materials are known to undergo severe stress during HBr curing due to the influence of strong VUV fluxes. The applied external stress will break the equilibrium between the three interfaces and lead to an unstable energetic situation. The system will therefore search to relax the applied stress and recover the initial stable configuration. Thus, the PR pattern sidewall will be displaced until all the forces are balanced and the system equilibrium is recovered. **In conclusion, the reflow can be defined as a PR/Air interface movement occurring to relax the increased residual stress. The surface tension acting on an interface enables the resist flow on a free surface, which will continue until the system recovers the equilibrium.**

There are many parameters that influence the reflow. In particular, it depends on the PR mechanical and thermal properties which depend on the polymer structure and physico-chemical nature.

III.2.2.1 Structural properties

The mechanical and thermal properties for any polymer result from the polymer chemical structure and the Molecular weight (MW).

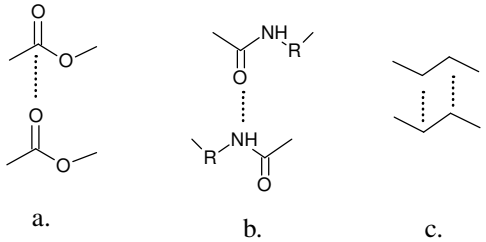

Figure III-11 Intermolecular forces in polymers: (a) Dipole-Dipole interactions, (b) H-bond interactions and (c) Van deer walls interactions.

Polymer chains are linked to each other by attractive forces such as, dipole-dipole forces, Van-deer-Walls or Hydrogen bonds (Figure III.11). These forces are responsible for the polymer matrix cohesion and they control the material viscoelastic behavior. The mechanical properties of a polymer are defined by the way in which polymer chains are linked between each other, and the facility to break/reform the linkages that gather the polymer chains together. Thus, the higher number of attractive forces between the polymer chains or if these forces are from a different nature that makes them be stronger (dipole-dipole, H-bonds…), the harder it will be to take these polymer chains apart, and therefore, the material mechanical properties will be different.

Typically, the number of attractive forces between the polymer chains is defined by the polymer molecular weight (i.e. the longer the chain, the higher probability to form a linkage), while the nature of these forces is defined by the polymer chemical composition.

Concerning our 193nm photoresists with different reflow tendency, both are methacrylate based resists with similar MW distribution. No relevant information concerning polymers chemical structure was provided by the supplier. However, the FTIR analyses shown in Figure III.8 have shown that the chemical structures of both resists are quite similar

III.2.2.2 Thermal properties

The thermal properties of a material consist in the behavior it presents when heating. In the case of a photoresist polymer, two main magnitudes are defined, the glass transition temperature (Tg) and the degradation temperature (T_d).

The glass transition temperature (Tg) is the temperature at which the molecular motion is high enough to make a polymer lose its glasslike properties and becomes rubbery-like. Although the Tg measurement is quite approximate (it varies strongly with heating condition, measurement repeatability, polymer uniformity, film uniformity…), anything that may increase the polymer molecule rotation decreases the Tg temperature.

Thus, polymer chemical structure becomes the main contributor for Tg modification. For example, high MW, presence of bulky pendant groups or backbone chain stiffening compounds (i.e. benzene rings) tend to increase a polymer Tg. Other contributions such as group polarity, presence of alkyl radicals (which may act as plastisizers) or polymer aging can also change the material Tg values. [25]

Glass transition temperature is a reversible phenomenon where polymer chemical structure is not modified. **However, when referring to polymers exposed to strong VUV fluxes (i.e. HBr cure) the polymer structure is changed during the cure process. According to the literature, this changes in the polymer chemical structure lead to a decrease of the polymer Tg values** [7]. Dynamic Mechanical Analysis (DMA) carried out over Resist A and Resist B (not shown here) confirm this hypothesis.

The polymer deprotection (or degradation) temperature (Td) is considered as the temperature at which the pendant groups linked to the polymer backbone are cleaved from the main chain. This cleavage is a non reversible reaction that leads to a certain amount of polymer mass loss.

To determine the Td of our polymers, the “thermogravimetric analysis” (TGA) was carried out. For this, photoresist films coated onto Silicon wafers were exposed to HBr cure conditions. Then the PR films were scraped off the silicon wafer and analyzed using the TGA technique. For further detail concerning the TGA, refer to Chapter II. The thermographs obtained after full TGA analysis for both resists (“Resist A” and “Resist B”) are shown in Figure III-12.

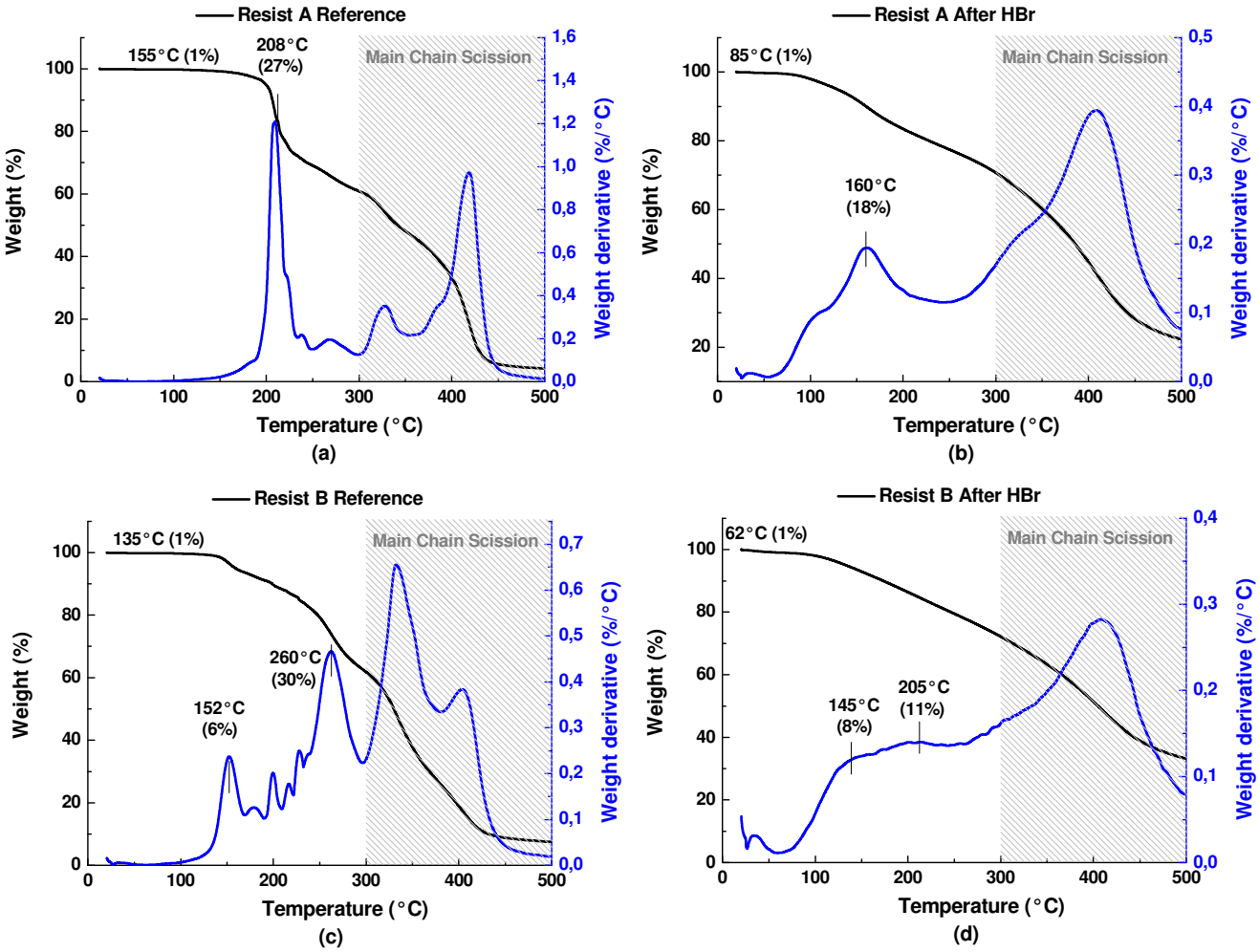

Figure III-12 TGA thermographs of "Resist A" (a, b) and "Resist B" (c, d) photoresist with and without HBr cure

Before HBr cure "Resist A" is degraded at higher temperatures compared to "Resist B" which suggests that "Resist B" is more sensitive to the temperature.

Pristine "Resist A" degradation reaction starts around 155°C, with a 1% mass loss that is attributed mainly to remaining solvent evaporation. The thermograph presents a major weight drop at 208°C (27% mass loss) which is attributed to the outgassing of the protective group (Fig III.12a). In "Resist B", degradation reaction starts at lower temperature (135°C, 1% loss due to solvent evaporation). Then, the TGA of resist B presents several peaks between 152°C and 260°C (36% mass loss) that may correspond to the outgassing of the 6 different pending groups attached to the main chain (Fig III.12c). **It is observed that the outgassing of protective groups occurs at lower temperatures for Resist B than for resist A (152 vs 208°C).**

After exposition to HBr cure conditions, degradation of photoresists occurs at lower temperatures. The polymer out-gassing starts at quite low temperatures around 85ºC (1% mass loss) for "Resist A" and 62°C (1% mass loss) for "Resist B". Then, the polymer degradation continuous gradually over a large temperature range until the major thermal degradation peaks appears at 160ºC and 145ºC-205°C respectively (Fig III.12 b and d).

Two hypotheses could explain the reason for which cured resists are thermally degraded at lower temperatures than reference resists:

- Some of the pendant groups that are cleaved from the main chain during the HBr cure remain within the resist film and are subsequently out-gassed during the TGA experiment at lower temperatures.

- The PAG present in the resist is activated by the VUV radiation emitted by the HBr plasma and the temperature ramp of the TGA analyses allows its diffusion and reaction with the protecting groups still attached to the polymer main chain. The presence of acids catalyzes the deprotection reactions and allows the pendant group cleavage at a lower temperatures than in a pure thermal deprotection reaction. It is as if the temperature ramp used for the TGA analyses plays the role of the post exposure bake (PEB) step of the lithography process

Thus, cured photoresists are likely more sensitive to reflow compared to reference photoresists because of their lower Tg and Td. **From these observations we assume that the PR thermal degradations occur at considerably lower temperature when the PR is previously exposed to an HBr cure treatment.** Particularly, for "Resist B" the PR degradations occur at temperatures around 60-70ºC. This easier thermal degradation of "Resist B" may explain the higher flowing tendency of this polymer as compared to "Resist A". For "Resist B", cure processes operating at 40-50°C may be sufficient to activate the PAG deprotection mechanisms and induce reflow(i.e. PEB for "Resist B" is carried out at only 70°C).

III.2.2.3 Mechanical properties

Polymer mechanical properties depend on the polymer structure, MW, crystallinity and crosslink density and therefore they will be different for amorphous, crystalline or cross-linked polymers. The 193nm photoresists consist of amorphous type polymers whose mechanical properties are driven by the MW and the temperature increase.

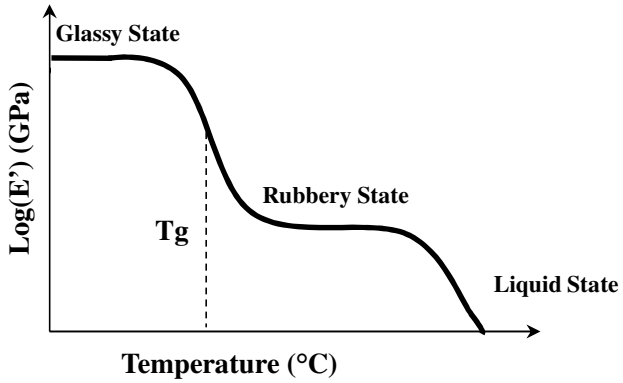

Figure III-13 Polymer mechanical properties as a function of temperature

Figure III. 13 represents the evolution of an amorphous polymer elastic modulus with temperature. At low temperature, polymers present a typical glassy state. As the polymer is heated, the kinetic energy of the polymer chains increases and the attractive forces keeping the chains together start to break (and reform). **At a certain temperature, the greater molecular motion leads to an increase free volume and the polymer loses its glasslike properties and becomes rubbery (Figure III.13). This temperature is relative to each polymer material and is known as the glass transition temperature (Tg).** At this temperature, the increased polymer chain motion allows chain reorganization in a more organized structure (i.e. polymer densification). With further heating, the

polymer will eventually lose its elastomeric properties and flow. In general we consider that if the processing temperature is higher than polymer Tg film densification may occur but if process temperature is higher than the polymer deprotection temperature (T_d) then resist will flow [22].

If, Tg < T Film densification

If, Td < T Resist flow

Another property that should also be considered is the polymer viscosity (η), or the resistance of the material to flow. In polymer chemistry, the viscosity can be defined by the following equation:

$$\tau = \tau_c + \eta\gamma \qquad \text{(Eq. III.2)}$$

Where, τ is the shear stress, τ_c is the critical shear stress required to initiate flow, and γ is the shear rate or the rate at which molecules flow relative to each other.

If we consider the flowing mechanism shown in Figure III.10, the polymer viscosity can be pictured as the force that counteracts the polymer flowing, and therefore, the lower the polymer viscosity, the more the material flowing (Figure III.14).

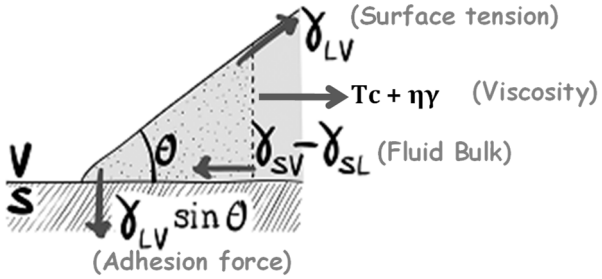

Figure III-14 Schematic representation of the resist flowing mechanisms considering the polymer viscosity

This property is actually dependent on the polymer's MW and temperature (Figure III. 15).

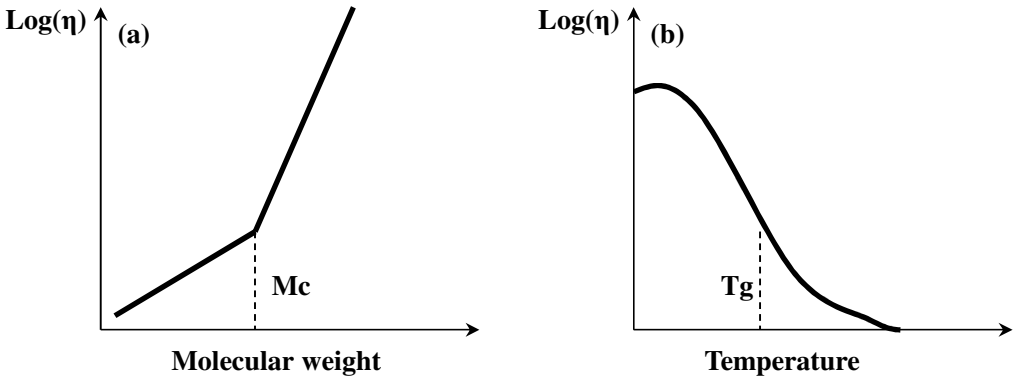

Figure III-15 Representation of the viscosity (η) of a polymer as a function of temperature [25]

Figure III. 15 shows the evolution of the polymer viscosity (η) with the molecular weight (Figure III. 15a) and the temperature (Fig III. 15b). Concerning the MW (Fig. III 15a), for short polymer chains the polymer viscosity barely changes with molecular weight. Over a certain MW (known as critical molecular weight "Mc") the polymer chain tends to turn around and create "knots" where the molecular motion is limited. For higher MWs the polymer viscosity is strongly increased.

Concerning the temperature (Fig III15b), the viscosity of a given polymer decreases with increasing temperature. Due to the increased polymer chain mobility a strong viscosity drop is observed around

the glass transition temperature (Tg). A lower viscosity results in a lower resistance to flowing. The polymer chains easily slip and therefore, it leads to higher reflow rates.

Therefore, we could assume that if VUV exposure results in a polymer chain scission mechanism, the MW of the polymers composing our photoresist may be reduced during the HBr cure treatments. Moreover, the cured resists present lower Tg values and are more easily thermally degraded. Consequently, it is expected that the viscosity of the HBr cured polymers should be lower, which could explain the observed resist flowing. We think that the propensity of a resist to reflow mainly depends on its thermal properties after cure treatment: the more sensitive to temperature degradation, the more likely to reflow. Moreover, it could have been interesting to evaluate the viscosity of our polymers before and after HBr cure. This would help us to confirm that the polymer viscosity has been considerably decreased by the cure treatment, and that resist B shows lower viscosity than Resist A, which could explain its significant flowing behavior.

III.2.2.4 Bulk effect

Together with photoresist chemical structure and mechanical properties, pattern dimensions may also impact resist flowing. Actually, *Lee et al* proposed a model to describe the flowing phenomena considering pattern adhesion to substrate and pattern size [26]. It was found that, the amount of polymer available to flow strongly impact the flowing rate. In this section, the impact of lithography pattern aspect ratio on resist flowing is studied. For this, gate features with different aspect ratios were obtained by varying the pattern CD from 30nm to 70nm and the resist thickness from 100nm to 120nm.

Figure III.16a shows the "Resist B" reflow as a function of initial pattern CD for various film thicknesses (100nm, 110nm and 120nm). Pattern reflow presents two regions with different behaviors depending on initial CD values. For initial CD values below 50nm, reflow seems to increase with larger CDs. In revenge, for initial CD values above 60nm, this tendency is inversed and the larger the CD, the lower the resist reflow.

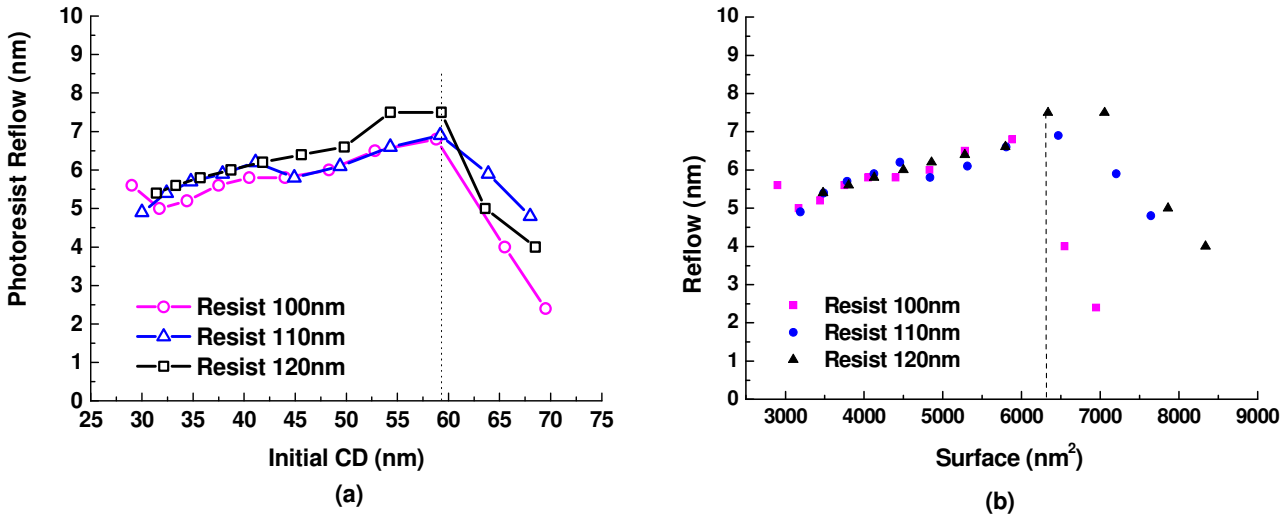

Figure III-16 Photoresist reflow as a function of (a) initial CD and (b) resist surface (pattern CD x Height) for various photoresist film thicknesses (100nm, 110nm and 120nm). The metrology error in CD values is considered to be +/- 0.4nm.

In Figure III.16b, the same data from Figure III.16a are plotted as a function of resist volume per unit length (CD x Height). As observed, the same two regions as in Fig.III.16a can be defined depending of their flowing tendency. For the first region, it is clearly observed that reflow is directly correlated to the resist volume available to flow. For the second region, corresponding to larger CDs some other mechanisms are taking place.

The behavior observed in the second range (CD≥60nm) may be attributed to many contributions. Firstly, it could be possible that larger patterns are less modified by cure plasmas. Secondly, the larger the pattern surface, the stronger the adhesion force towards the substrate is, which may reduce the resist flowing. And finally, another explanation can be proposed considering the stress relaxation mechanisms. In larger patterns the stress relaxation may preferably occur in the volume by increasing chain mobility along the pattern length rather than along its width. Therefore, the bigger the pattern (large CD) the lower flowing is observed.

In conclusion, pattern dimensions and aspect ratio impact resist flowing. **For small patterns (CD≤60nm) constraint relaxation results in a displacement of the surface boundary and results in a resist flowing where the reflow is driven by the amount of polymer available to flow. In revenge, for large patterns (CD≥60nm), there may be a combination of the increased adhesion force with larger width and the stress relaxation along the pattern length that slows down the resist reflow.** This fact may also be the reason for which no resist flowing has been observed for older 193nm photoresists, where larger pattern CDs were targeted.

III.2.2.5 Conclusion

During HBr cure steps, polymer main chain scission, pendant group cleavage and degradation of lactone and ester groups occurs. These modifications result in polymers with a different chemical composition, lower MWs, lower Tg values and lower viscosities which are also more sensitive to thermal degradation. These changes lead to an increase of the polymer chain mobility and a modification of the polymer physico-chemical behavior. All these modifications change the surface tension and break the equilibrium that keeps the PR pattern stable.

Thus, the PR pattern sidewall boundary needs to be displaced in order to recover the equilibrium and the resist reflow occurs. **The reflow is then a competition between the surface tension, viscosity and polymer adhesion force and it will stop when the system equilibrium is recovered.**

The reflow is then dependent on the polymer structure, physic-chemical nature and thermal and mechanical properties and is proportional to the volume to be reflowed.

III.2.3 Pattern deformation mechanism

Although the resist flowing phenomena is well known, the deformations mechanism observed over 2D patterns are harder to describe. To relax this increased residual stress, the PR patterns reflow and lead to a 2D pattern deformation that cannot be corrected at lithography level.

Some authors attribute the deformations observed over resist films to the formation of a capillary wave [27] [28].*K. Kenyon et al*, based on the theorems developed by A. Einstein in 1916, described a capillary wave as a wave that propagates at a phase boundary of a fluid and whose dynamics are dominated by the surface tension effect. Thus, following this assumption, surface tension acts like a restoring force that will try to uniform the volume differences in the surface of a fluid (i.e. flatten the bulges in a curving surface). This suggests that in a 2D pattern the fluid may flow from the sites with small PR volumes towards the sites with high PR volumes. When looking to the deformations observed in our 2D patterns,

this assumption seems to be possible (Fig. III.17). However it is most usually used to describe macroscopic fluid systems and may not be adapted to describe flowing in nanometer scale resist patterns.

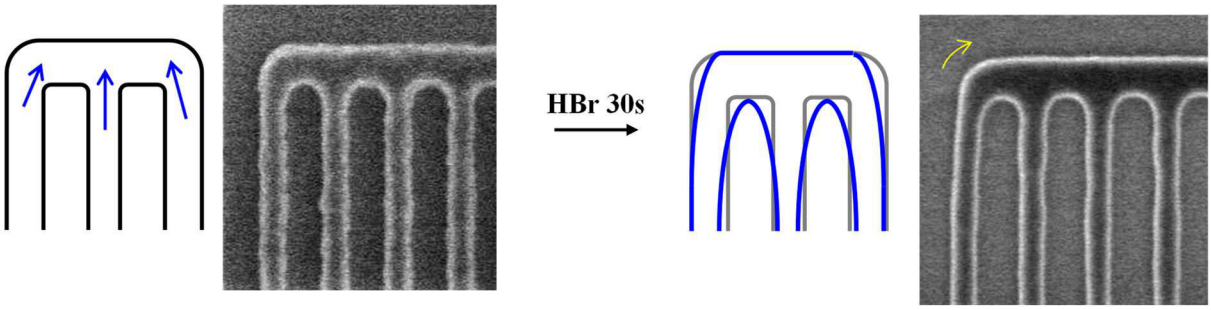

Figure III-17 Comparison of schematic drawings of pattern deformations following the capillary wave theory with real pattern deformations observed by CD-SEM

Other authors also refer to the unbalanced surface stress as the origin of the polymer deformations [29].*B. Heise et al*, proposed a method to spatially measure the stress differences within polymer structure. Figure III-18 proposes the stress differences measured over a polyethylene polymer bar which was curved onto a bent structure. Their measurements showed that the polymer present a tensile stress at the top of the bow while a compressive stress was measured at the bottom of the bow.

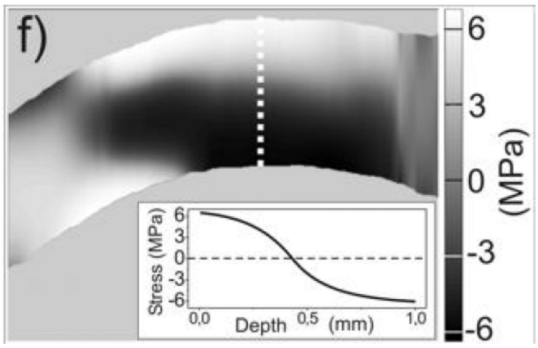

Figure III-18 Stress image of a LDPE polymer bar bent into a curved structure. Inset: Stress profile along the dotted line [29]

This work suggests that there is a resulting residual stress generated only by photoresist pattern structuration. Depending on the 2D structure given to the PR pattern, the residual stress present in the PR pattern will not be the same from one structure to another and will also be non-uniform within a same PR structure. These residual stresses may influence the way in which the unstable system will recover its equilibrium and may then influence the pattern deformation.

In any case, besides from this internal stress generated due to pattern structuration, we know that during cure process, additional residual stress is accumulated. The cure treatments induce polymer physico-chemical modifications that lead to a resist flowing, that is dependent on the amount of matter available to flow. In a 2D pattern, the photoresist distribution is not uniform within the full structure, and therefore, the resist flowing is also assumed to be non-uniform. Due to this reflow non-uniformity, an irregular pattern deformation is observed in 2D structures.

In conclusion, the pattern deformation observed in 2D patterns and referred as gate shifting is most likely due to the combination of an unbalanced surface stress and a non-uniform resist flowing. If the resist flowing observed on PR lines can be easily corrected by addition of optimized trim

steps, pattern deformations observed in 2D structures cannot be addressed by trimming. Gate shifting needs to be solved by a specific optimization of gate etch process.

III.3 Towards gate shifting improvement

From now, only resist B has been used for the results shown below

III.3.1 Metrology

In order to evaluate the efficiency of our process to correct the gate shifting, a proper metrology needs to be developed. While the LWR is typically measured over line patterns (See Chapter II-section II.3.2.3), gate shifting is basically observed in logic 2D structures. Therefore, 2D patterns are chosen for the development of a proper gate shifting metrology. *T. Wallow et al*. previously proposed a Finite Element Analysis (FEA) simulation method to estimate cure induced photoresist corner rounding [19].However, in-line metrology was preferred for this work. Because other metrology techniques such as overlay cannot measure deviations in this type of structures, CD-SEM measurements have been used (Figure III-19) to evaluate pitch changes (CD_{line}+CD_{space}) and thus pattern shifting.

First, pitch measurements are done in those pattern positions where the contacts will be placed lately (Fig. III.19a). Then, the pitch values measured after lithography are compared to those obtained after full etch. A comparison of both measurements is plotted in Figure III-19d. Column bars represent the pitch value measured at each measurement point after lithography and after full etch. For confidentiality reasons, the pitch values cannot be given. However, Figure III-19d is plotted at scale and the relative variation between each bar is correct and given by the y axis. CD-SEM measurements done over photoresist patterns (Figure 19b), show constant pitch values at the four different measurement points. However, pitch measurements after full etch show some variability from one pitch to another. Pitch4 location remains unchanged after etch process while pitch2 location is the most impacted one. Therefore, the pitch value difference between position 2 and position 4 seems a fairly good estimation of the pattern shifting after a given etch process (represented by the dotted line).

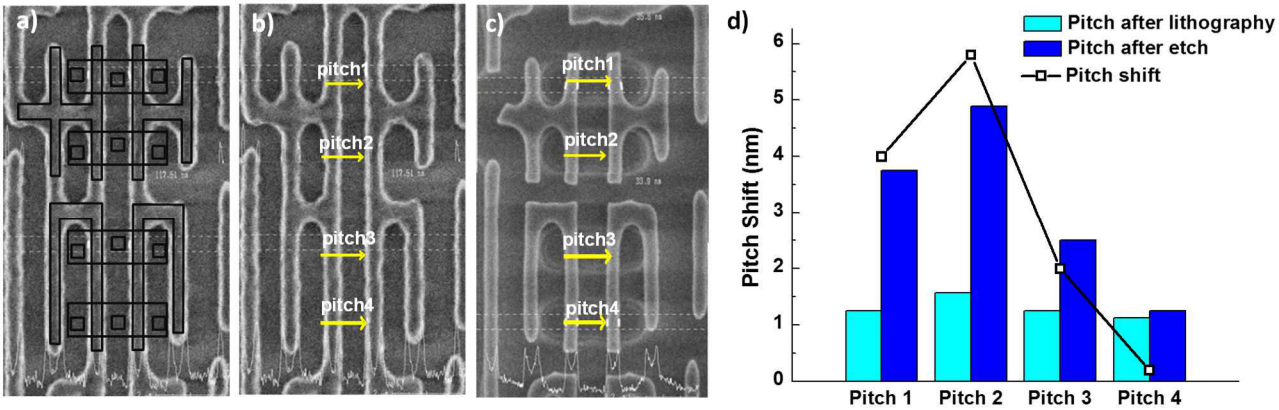

Figure III-19 (a) Reference structure used to monitor gate shifting. Planar description of the gate-contact position is shown together with CDSEM pitch measurement locations (b) after lithography and (c) after etch. Pitch measurement data is represented in graph d).

As it has been explained in the previous section, if resist flowing is considered as the main root cause for the pattern shape deformations, differences between pitch values can be explained. Indeed, the reflow process during HBr cure is assumed to be isotropic and dependent on the amount of polymer available to flow. Consequently, the reflow will be more accentuated nearby concave corner, explaining why pitches 2, 3 and 1 are more impacted than pitch 4 (Figure III-19d).

If gate shifting as well as CD increase both derive from resist flowing, there should be a correlation between both parameters. Figure III.20 shows the correlation between the observed CD increase measured in a dense array of lines and the gate shifting measured in 2D patterns. **Hence, the larger the CD increase, the stronger the gate shifting effect.**

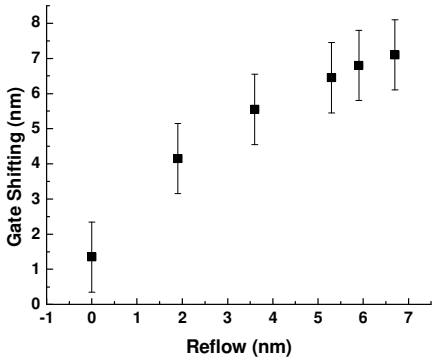

Figure III-20 Correlation between in line CD vs GS measurements

Still, we need to remain careful on this assumption. A CD increase does not systematically mean presence of gate shifting. Some etch processes such as trim, increased deposition or hard mask erosion can modulate CD values but do not largely impact gate shifting.

III.3.2 Impact of HBr cure plasma parameters on gate shifting and LWR

It seems that to preserve the LWR, a cure step is mandatory but needs optimization to avoid pattern shifting. As already mentioned the resist reflow during HBr cure is the main contributor to pattern shifting and consequently needs to be minimized. **The reflow is due to the VUV induced chain scission and could be controlled by limiting the HBr plasma VUV dose. To control the emitted VUV dose, there are two possibilities; either we limit the exposure time, or the emitted VUV flux.** Let's look first at the impact of the exposure time.

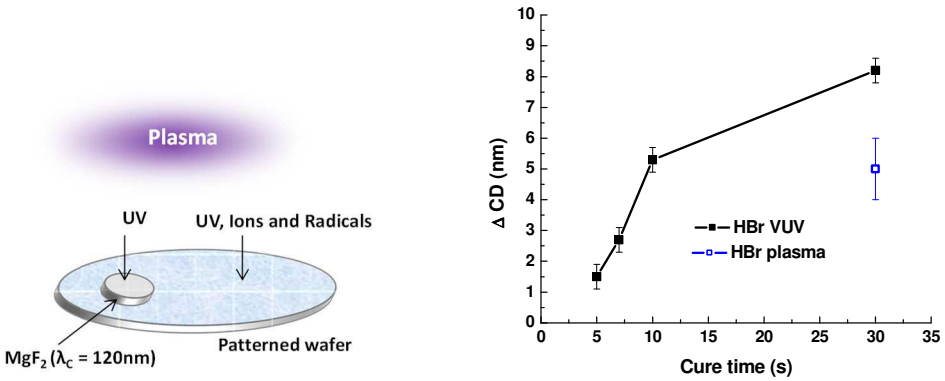

Figure III-21 Photoresist CD line evolution with HBr plasma VUV exposure time (patterns were exposed to 1320ws HBr plasma through MgF_2 windows) A schematic representation of the protocol used for this experiment is also shown.

The impact of the VUV dose on the CD of "Resist B" patterns exposed to HBr plasma have been investigated by CD-SEM measurements as reported in Figure III.21. To decorrelate the contribution of plasma VUV irradiation from the plasma itself (presence of ions and reactive species and VUV), the

protocol reported by *Pargon et al* was used [6]. This consists in placing a MgF_2 window on the patterned wafer during the HBr plasma exposition (cf. Figure III-21). The window will act as a plasma VUV high pass filter with a cutting wavelength of 120nm and will shield the resist patterns from ions and radicals. Figure III-21 shows that the CD of the resist patterns placed under the MgF_2 window (noted HBr VUV in Figure III-21) rapidly increases during the first 10s of VUV exposure, and above 10s the CD increase is more moderate.

FTIR analyzes have also been carried out on resist B blanket wafer exposed to HBr plasma (with and without MgF_2 window in place) for two processing times, 7s and 30s (cf. Figure III-22).

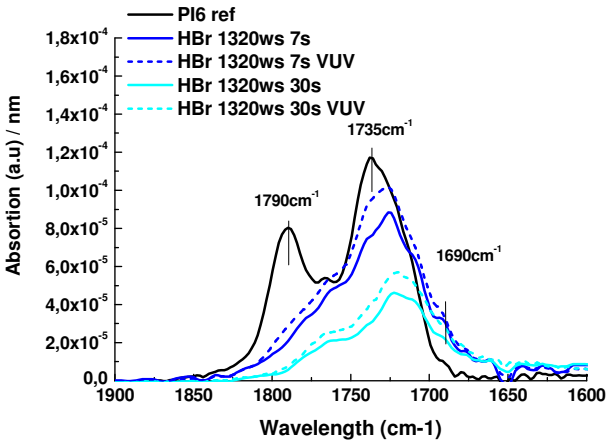

Figure III-22 C=O region FTIR spectra of a photoresist exposed to an HBr cure (Full plasma and VUV) at 1320w during 7s and 30s

FTIR analyses confirm what was already observed by other authors: VUV irradiation is responsible for the chemical modification induced by HBr plasma treatment, which consists in photolysis of ester and lactone groups at $1790cm^{-1}$ and $1735cm^{-1}$ and the formation of acids (peak at $1690cm^{-1}$). After 7s of plasma exposure, the lactone group has already been completely decomposed, while the ester group is degraded at a slower rate. Consistently with other studies [6] [30] [7], we observe that the main chemical modifications induced by cure treatments occur very rapidly during the first 10s of plasma exposure. The resist is further modified for longer exposure times but at a moderate rate. Those preliminary results confirm that VUV plasma irradiation induce some chemical modifications within the resist that are certainly responsible for the resist flowing, and that the kinetics involved are almost instantaneous. For comparison, the resist CD increase measured after exposure to 30s of HBr cure full plasma is also reported in Figure III.21. It is observed that the CD increase with HBr plasma is less significant than the one obtained with 30s of VUV irradiation. This is consitent with previous studies, that suggest that a C-rich layer is formed on the resist pattern surface during HBr plasma exposure and limits the resist reflow [2] [5].

To confirm this hypothesis, we have measured the thickness of the carbon layer that is formed on the resist surface using the experimental protocol described in Figure III.23a. A sample composed of Polysilicon features obtained by classical top down approach (lithography+plasma etch+ wet to remove hard mask and residues) has been patched on a blanket photoresist wafer. The wafer is then exposed to HBr cure plasma process at several processing times. After HBr plasma, the silicon patterns are characterized by TEM .

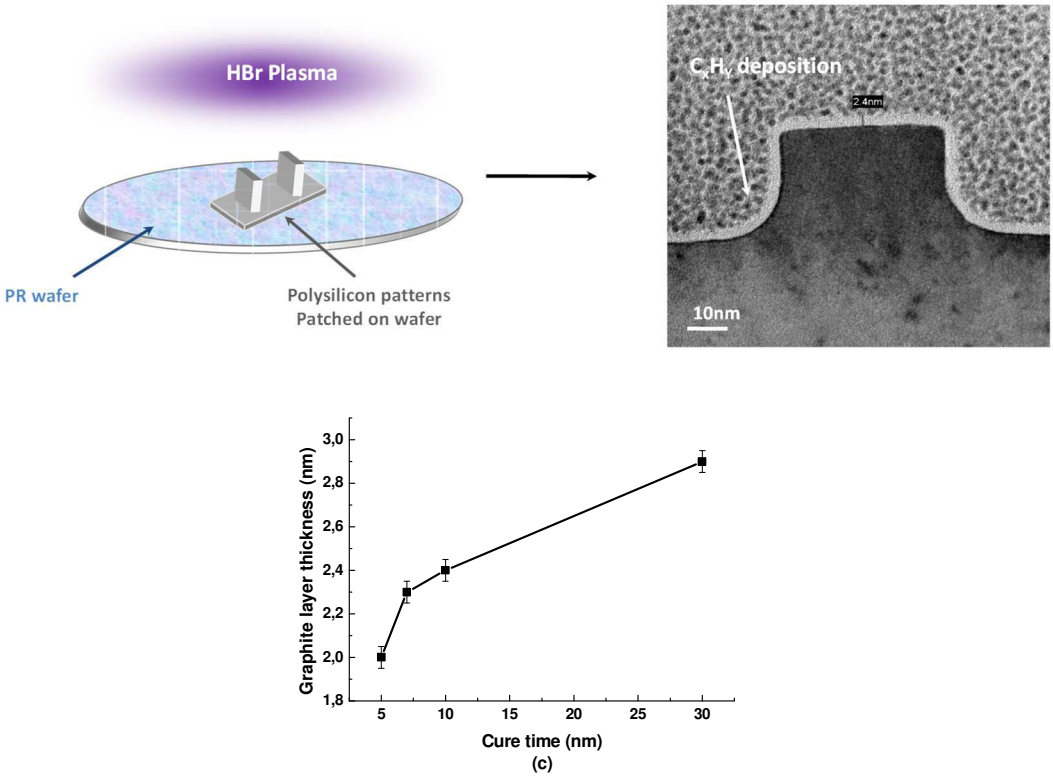

Figure III-23 (a) Schematic representation of the set up for the determination of the carbon deposition thickness; (b) TEM image of the silicon pattern after HBr cure plasma exposure of 10s where a conformal deposit of 2.4nm is observed (c) Carbon deposition thickness with cure time.

It is observed in Figure III.23b that a conformal deposit of about 2.4nm has been formed on the silicon pattern after a 10s HBr cure. We assume that the deposit formed on the polysilicon patterns is similar to the one that forms on the photoresist patterns during the HBr cure and comes from the redeposition of the carbon byproducts that are outgassed from the resist during the cure treatment. The carbon deposition thickness has been measured for several cure processing times as reported in Figure III-23c. It is observed that after 5s, a 2nm carbon layer is already formed on the silicon patterns and grows slowly with the plasma exposure time, reaching 2.8nm after 30s processing time. For longer exposure times this thickness is known to saturate and remain stable [5]. The kinetics involved in the carbon layer formation during HBr plasma processing seem to be instantaneous. **However, these experiments show that there is a competition between polymer reflow and the formation of the carbon surface layer deposition. It seems that the resist flowing kinetics are higher than the Carbon deposition kinetics and therefore, the carbon deposit could limit the reflow but not suppress it.**

By decreasing the HBr processing time down to 7s, the resist CD increase could be limited to values inferior to 3nm (Fig III.21), which lets us consider that an improvement of the gate shifting can be done. Unfortunatelly, we do not have enough information to conclude, it would be necessary to measure the CD evolution with cure time (5, 7, 10 and 30s) during a full HBr plasma process (Noted as HBr in Fig. III.21). Two different situations are possible. Either the CD increase by UV exposure and HBr exposure is the same for lower cure times (CD_{VUV} = CD_{HBR} at t<15s), which suggest that the reflow cannot be controlled by the deposition of dense carbon layers, and the resist lines will reflow at least 5nm (in 10s). Or, the CD increase after full HBr exposure is always lower that the CD increase under VUV

exposure only (CD_{HBr} < CD_{VUV} for any cure time). In this case, we can consider that the carbon deposition limits the resist reflow; thus, working at low HBr cure times (5 to 7s) could avoid the reflow and therefore gate shifting phenomenon. However, such a short processing time is not an industrial solution for plasma reproducibility, and this option cannot be considered.

Another option that was evaluated was to tune the source power in order to tune the VUV flux. Decreasing the source power leads to a lower molecule excitation and therefore a decreased VUV emission. Due to the lower VUV emission, the VUV dose absorbed by the polymer for the same cure time will be lower and the polymer matrix will be less impacted. FTIR spectra in Figure III.24b confirm this assumption. At lower source power, lactone opening (peaks at 1790cm^{-1} and 1735cm^{-1}) and acid generation (peak at 1690cm^{-1}) is observed but ester groups remain nearly untouched. The impact of the source power on the CD of resist B patterns exposed to HBr plasma is shown in Figure III.24a. As expected, the reflow decreases with decreasing source power and is even suppressed at a source power of 300W. In Figure III.24a, the evolution of the LWR as a function of the source power is also plotted. It is observed that a 4nm LWR is obtained for any source power, compared to a LWR of 5nm after lithography. It is known that the smoothening effect induced by VUV irradiation saturates above a certain dose [7] [30].

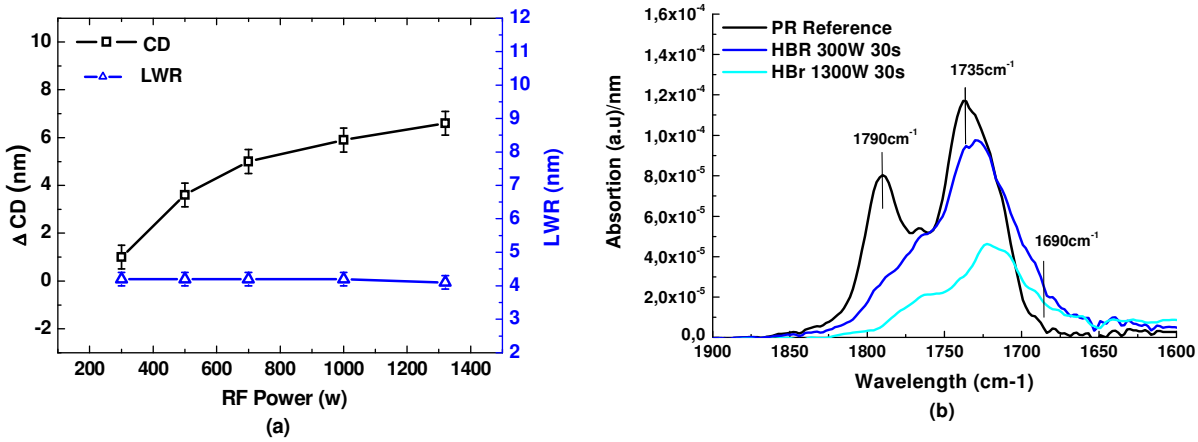

Figure III-24(a) CD and LWR evolution with applied source power in an HBr plasma. All plasma conditions except from source power are kept constant: Pressure of 5mT , 40°C, 30s. Initial resist LWR is ~5nm.(b) FTIR spectra of a resist exposed to HBr cure (1320ws and 300ws).

Another way to modify the VUV emission is to change the pressure conditions (Figure III.25). At higher pressures, the plasma density increases and the mean free paths for particule collission shortens. This results in a higher collision probability and higher particule excitation that leads to higher VUV emission. This increased VUV flux increases photoresist flowing of 2nm at higher pressures (HBr at 300w and 7mT). Since LWR smoothing mechanism is also dependant of VUV flux, increased VUV emission also leads to slightly lower LWR values at higher pressures. Thus, working at lower pressures could limit polymer reflow. At pressures around 2.5mT, no resist flowing is observed and LWR values remain acceptable. However, such low pressures reach the equipement working limits and are not stable to ensure process stability. Therefore, no pressure tunning is possible to limit resist flowing.

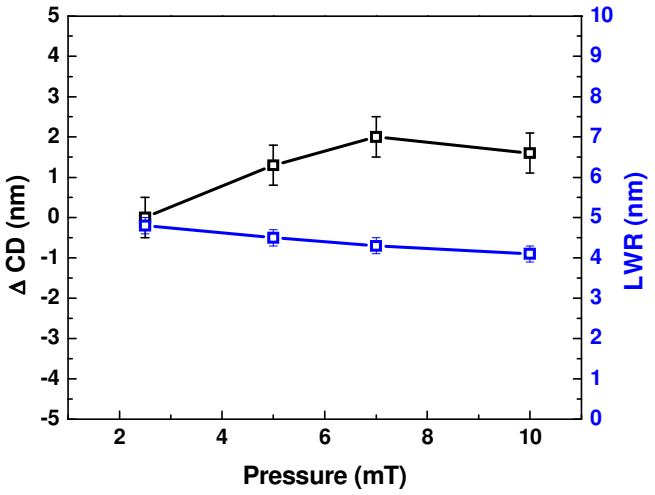

Figure III-25 CD and LWR evolution with applied pressure in an HBr at 300w and 40°C during 30s. Initial LWR of 5nm.

A last option to limit resist flowing is working at lower process temperatures to limit thermal degradation of VUV cured resists. Figure III.26 shows no CD increase dependance on chuck temperature. The resist surface temperature was measured to be 50°C when the chuck was set at 40°C. If a linear temperature increase is supposed, with a chuck at 50°C surface temperature should be high enough to start polymer degradation and increase flowing. The fact that no CD change is observed for a range of temperatures between 30-50°C in an HBr plasma at 300w source power suggests that the plasma conditions chosen for this experiment do not modify resist surface temperature largely.

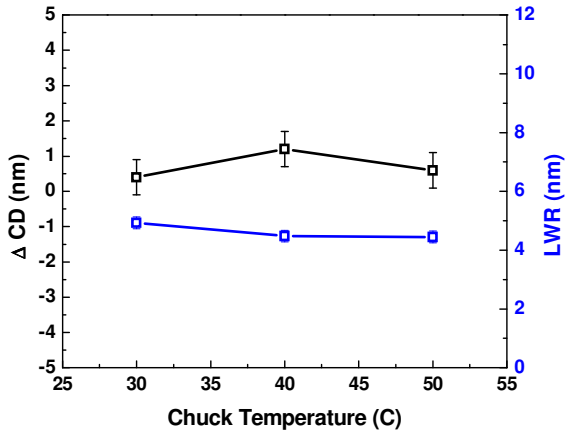

Figure III-26 Resist reflow as a function of the working temperature. Plasma conditions are HBr at 300w source power with a pressure of 5mT during 30s. Initial LWR of 5nm should be considered.

In conclusion, in order to control resist flowing, emitted VUV irradiation should be limited. For this, the VUV dose needs to be controlled, either by tuning the VUV flux by modification of plasma parameters or the VUV exposure time.

From our results, we can assume that:

- **Reducing the HBr cure process time is not convenient to suppress the resist flowing**
- **Reducing the working source powers helps us to control the emitted VUV flux, and therefore the resist flowing**
- **Working Pressure and Temperature do not have an strong impact on the resist flowing, at least in the Pressure and Temperature range studied.**

And therefore, we conclude that carrying out **HBr cure treatments at 300w during 30s is the best option to limit the resist flowing but keeping good LWR values**.

III.3.3 Impact of cure plasma chemistries on gate shifting and LWR

Another parameter to be studied is the cure plasma chemistry. Much work has been done to prove the ability of different plasma chemistries to smooth photoresist surface and improve etch resistance [2] [31]. However, in our case, we are interested on cure chemistries with limited VUV irradiation or different chemical reactivity to address both LWR and gate shifting. In this section, two plasma chemistries will be discussed as possible resist pretreatments: H_2 cure plasmas, and Cl_2/O_2 trim steps.

III.3.3.1 H_2 cure chemistries

H_2 based plasmas are good candidates to substitute HBr based plasmas due to their strong ability to smooth polymer surface [2]. The mechanisms driving this smoothing process are almost the same as in an HBr plasma. Actually, in H_2 based plasmas, the smoothing process is a combination of the VUV induced polymer photolysis and resist isotropic etching by reactive hydrogen radicals [30] [2]. H radicals will etch the photoresists by formation of CH_4 or H_2O and will also limit by-product recombination into sticky polymers in the gas phase [32] [33]. Thus, no deposition of carbon rich layers occurs in H_2 plasmas, and the LWR increase due to the formation of an instable double layer system is suppressed. Moreover, photoresist asperities (such as footing) will be equally etched by H radicals leading to smoother resist surfaces after full H_2 plasma processing compared to VUV irradiation emitted by H_2 plasma only [30] [2].

However, since, no protective C-rich layer formation occurs in H_2 cure steps, resist pattern stability may be compromised. In this section, we discuss the suitability of H_2 plasmas as photoresist pretreatments considering resist surface roughness and resist flowing.

Figure III-27 shows SEM cross section images of “Resist B” photoresists cured in HBr and H_2 based plasmas. Note that since photoresist etch rate in H_2 is higher than in HBr, cure time was decreased to 10s (instead of 30s) while other plasma parameters (power, pressure…) remain constant.

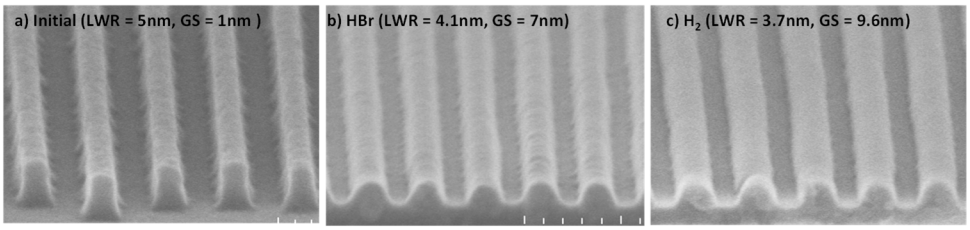

Figure III-27 SEM Cross-section images of "Resist B" patterns after: (a) lithography and exposure to (b) HBr plasma and (c) H_2 plasma. The plasma parameters are a source power of 1320w at 5mT and with chuck temperature fixed to 40°C. For HBr cure, 30s plasma treatment was chosen while 10s were used in H_2 cure. LWR values were calculated by CD-SEM.(CD-SEM uncertainty: ±0.2nm).

It is shown that after cure plasma treatment, photoresist roughness is decreased from 5.0nm to 4.1nm in HBr and 3.7nm in H_2. As already reported, H_2 cure treatment is more efficient to smooth the photoresist surface because no carbon redeposition occurs on the pattern sidewalls [2] [34].

However, resist patterns also present more rounded profiles suggesting a possible resist flowing. Analysis of resist line CDs by CD-SEM is shown in Figure III-28. Considering initial CD lines of ~46nm, under exposure to a 30s HBr cure resist lines increases of 6nm while 12nm CD increase is seen after 10s of H_2 plasma. This CD increase is then maintained during SiARC etching without further modification (1nm CD loss maybe observed due to photoresist erosion during SiARC etching).

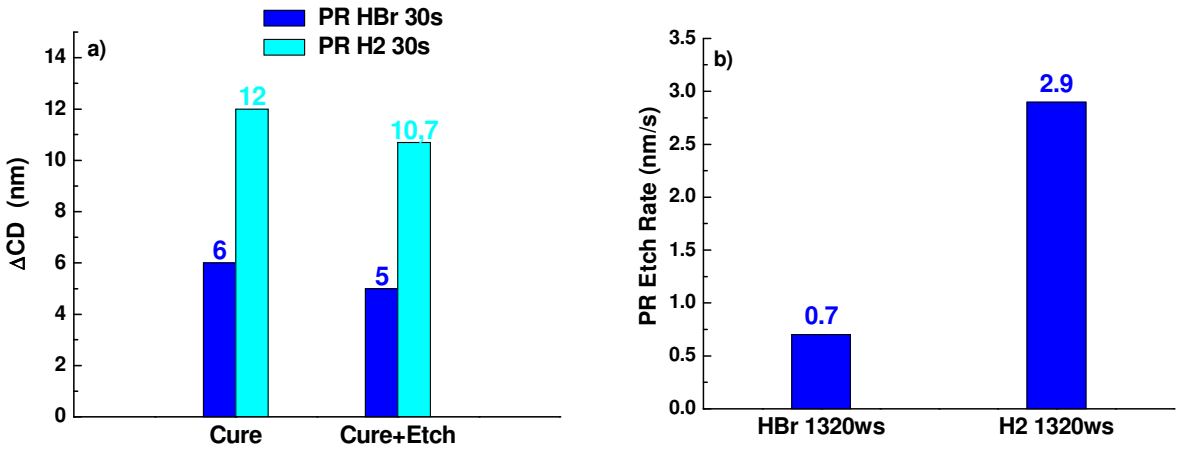

Figure III-28(a) CD variation of PR exposed to 10s H_2 cure and 30s HBr cure, and subsequently exposed to the SiARC etching process (b) Etch rates of photoresists exposed to10s H_2 or 30s HBr cure treatment

The photoresist etch rate measured on blanket wafers exposed to HBr plasmas during 30s is around 0.73nm/s while an etch rate of 2.9nm/s is measured for H_2 cured resists (Figure III.28b). In the case of HBr cure, the etch rate is mostly due to the photolysis and subsequent densification of the resist film. It has been shown that the thickness loss of photoresist films exposed to HBr plasma rapidly decreases with the HBr processing time and saturates above 60s. In the case of H_2 plasma, the etch rate is much more pronounced because H reactive radicals/ions also contribute to the etch rate. From this vertical etch rate trend, it is expected that H_2 plasmas could lead to lateral erosion of the photoresist during the H_2 cure treatment. However, it is observed in Figure III.28a

that the photoresist pattern CD increases of 12nm during H_2 cure suggesting that the reflow mechanisms dominates over the lateral etching by H radicals. The absence of hard carbon layer on the photoresist patterns exposed to H_2 cure could explain the significant reflow obtained compared to HBr cure However, it should be noticed that the CD increase obtained after 10s H_2 plasma (12nm) is higher than the one obtained after 10s or even 30s of HBr VUV exposure (5nm and 8nm respectively, cf. Figure III.21b)

A factor that may change from HBr plasmas to H_2 plasmas is the emitted VUV flux. Titus et al [35] [36] demonstrated that the VUV flux towards the substrate surfaces could be estimated by monitoring the chemical changes in 193nm PR induced by VUV exposure using FTIR absorption spectra. Indeed, they showed that the FTIR peaks for the C=O bonds in the 1700-1800cm-1 region decrease only as a function of VUV dose and suggests that this measurement can be utilized as a chemical dosimeter. Figure III-29 shows the FTIR spectra of "Resist B" exposed to either HBr or H_2 plasmas. The process conditions are the same for both plasma chemistries except from process time (30s for HBr and 10s for H_2). The FTIR spectra of the same resist exposed to an HBr plasma during 10s is also shown to help the interpretation.

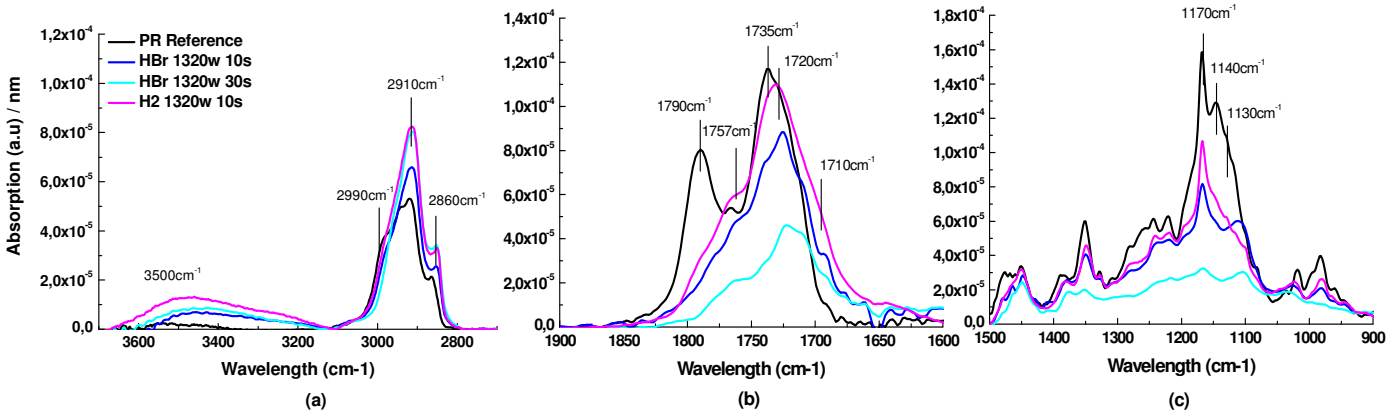

Figure III-29 FTIR spectra of a resist exposed to HBr (30s and 10s) and H_2 (10s) cure treatments. Plasma conditions were 1320ws, 5mT, 40ºC for all spectra.

The chemical modifications induced by H_2 plasmas are similar to those observed with HBr: the lactone group is mostly degraded (loss of C=O peaks at 1790cm^{-1}, Fig III.29b), but contrary to HBr, the ester groups are almost not impacted after 10s process (no loss of C=O peak at 1720cm^{-1}, Fig III.29b). The loss of COC peaks at 1140-1130cm^{-1} (Fig III.29c) observed with H_2 plasmas is mainly attributed to the degradation of the lactone group, while in the case of HBr the more pronounced COC peaks decrease is also due to the cleavage of the COC bond related to the ester linking the pending groups to the main polymer chain. For both plasmas, the lactone (and ester) degradation is accompanied by a strong carboxylic acid formation (C=O peaks at 1690cm^{-1} and 1757cm^{-1} (Fig III.29b) and O-H band at 3500-3200cm^{-1}(Fig III.29a)). The formation of carboxylic acid seems to be slightly more important with H_2 than with HBr. Finally, the peak at 2990cm^{-1}related to the stretching of a methyl group adjacent to a carbonyl (or a O atom) decreases, while peaks corresponding to CH_2 stretching vibrations at 2860cm^{-1}and 2910 cm^{-1} seem to appear at higher intensities and shifted to lower wavenumber positions at 2845cm^{-1}and 2901cm^{-1} (Fig III.29a) suggesting the formation of a different CH environment.

Based on the work of Titus and comparing the signal intensity of the C=O bonds and COC in Figure III.29 (b&c), it can be assumed that the VUV flux emitted by H_2 plasma is similar or even slightly inferior to the one emitted by HBr plasma. This means that the VUV flux is not the only responsible for the increased resist reflow in H_2 plasma. As mentioned above, there is some slight differences in the FTIR spectra presented in Figure III-28 between HBr and H_2 plasma. The resist exposed to H_2 presents a more hydrogen saturated structure. This assumption is done from the increased emission of C-H bonds, O-H and COOH bonds due to the formation of carboxylic acids (COOH) and saturated aliphatic groups (CH_2)

In H_2 plasmas, there is a strong concentration of H radicals that are small and light enough to diffuse through the whole polymer matrix. Due to their strong reactivity, they will easily react with polymer pendant groups impacted by VUV exposure (i.e. opened or cleaved lactones) and form hydrogen saturated compounds (COOH, CH…). The higher mobility of H radicals compared to polymer chains avoids the formation of C-C bonds and the resulting polymer fragments will be smaller and less cross-linked. Thus, the resist chain mobility increases and resist flowing rate is higher. **In conclusion, a higher resist flowing is observed for photoresists exposed to H_2 plasmas compared to those exposed to HBr, for an equivalent photon flux. This increased resist flowing is attributed to the diffusion of hydrogen through the polymer matrix that reacts rapidly with free C radicals formed as a result of bond cleavage by the VUV irradiation. This leads to shorter and more mobile polymer chains which favors the reflow mechanism.** At this state, the most suitable plasma condition to obtain correct LWR and GS values is still an HBr cure at 300ws.

III.3.3.2 Cl_2/O_2 trim chemistries

Other possible candidates to improve photoresist line with roughness with controlled VUV emission are resist trim steps. Trim steps are chemically reactive plasmas, typically based in O_2 plasmas that will accomplish photoresist isotropic etching [37]. They were initially added into the gate etch processes to decrease resist CD values to target but they are also known to improve photoresist initial LWR. Their chemical reactivity is responsible for photoresist smoothing by reactive etching of resist asperities and non-uniformities [38].

Figure III-30 shows a comparison of photoresist patterns after exposure to 30s HBr, 10s H_2 cure plasmas and 40s Cl_2/O_2 trim plasmas. LWR and GS values were measured by CD-SEM and are also indicated on Figure III-29.

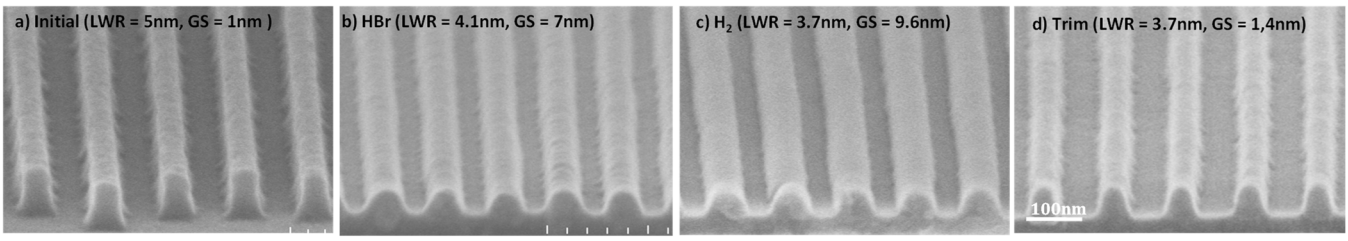

Figure III-30 SEM Cross section images of photoresist after (a) lithography, (b) 30s HBr cure (c) 10s H_2 cure and (d) 40s Cl_2/O_2 trim step. LWR and GS values were previously measured by CD-SEM.

After trim (Figure III-30d), the photoresist presents a more rounded profile but no particular resist flowing. Relatively low GS values were measured over top view CD-SEM images as compared to other cure treatments. Besides, a 40s trim leads to an equivalent LWR of 3.7nm as obtained for 10s H_2 plasma treatments. As no hard carbon layer is formed during the trim process contrary to the HBr cure, LWR

obtained after trim (and H_2) are lower than those after HBr cure. Similar smoothing mechanisms are then supposed for trim and H_2 treatments and based on the combined action of the VUV irradiation and the strong chemical reactivity of the H radicals (in H_2) and O radicals (in Trim) **In conclusion, by addition of trim steps, no resist flowing is observed, and good LWR values can be obtained without increasing the gate shifting phenomena.**

Figure III.31 shows main process parameter (Resist thickness, CD, LWR and Gate shifting) evolution with trim processing time.

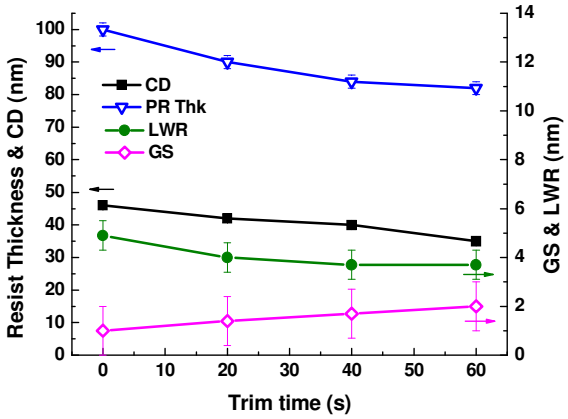

Figure III-31 Process parameter evolution (CD, resist thickness, LWR and gate shifting (GS)) with trim time.

Not surprisingly photoresist thickness and pattern CD decrease with trim time. The measured higher photoresist vertical etch rates (0.3nm/s thickness loss) compared to lateral etch rates (0.2nm/s CD loss) are attributed to the ion/radical synergy that takes place on horizontal surfaces while vertical surface etching is mainly driven by radical flux. Since an evident CD loss is obtained by resist trimming it is believed that with the trim plasma conditions used in this study, the reflow, if present, has very low rate and can be counterbalanced by the lateral etching induced by plasma radicals. Consequently, the gate shifting values remain very low (below 2nm) for any trim process durations (Fig. III 30). The slight increase in the Gate shifting observed with trim time may be attributed to the non-uniform lateral etching of 2D patterns due to different shadowing effects.

Concerning the LWR, it decreases from 4.9nm to 3.7nm during the first 30s of process and then stabilizes for longer trim times. As already mentioned this smoothening is partly due to VUV irradiation emitted by Cl_2/O_2 plasmas. As shown in the FTIR spectra in Figure III- 32, photoresist films exposed to Cl_2/O_2 plasma undergo similar chemical modifications as HBr cured resist but the kinetic loss of lactone and COC bonds is much slower than for H_2 or HBr cure treatments, suggesting that the VUV flux is much lower in trim process conditions.

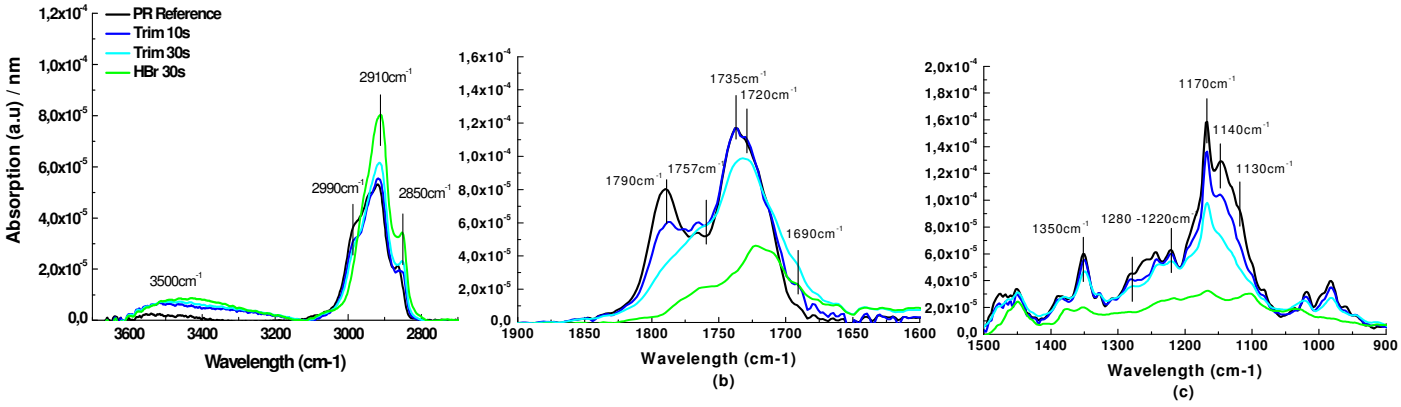

Figure III-32 Comparison of FTIR spectra of (a) OH and CH stretching regions, (b) C=O region and (c) COC stretching region of a photoresist after exposure to trim steps (7s and 30s) and HBr cure steps.

This suggests that another mechanism drives the resist smoothening in trim plasma. *Rauf and al* [39] suggested that the rough protrusions (referred as positive roughness) on the resist sidewalls get exposed to energetic ions at grazing incidence, and are removed through physical sputtering. Simultaneously, the incoming flux of etching species (mainly atomic oxygen) into the rough indentation (referred as negative roughness) on the PR sidewalls is slightly reduced due to shadowing effect, which lowers the etch rate at the rough identation. *Rauf et al* conclude that this disparity in etch rate of positive and negative roughness contributes to the smoothing of the PR sidewalls during the trim etch process. Like us, they also observed that the smoothening effect of resist trimming plasma is not linear with process time, and tends to saturate. In fact, when the roughness size becomes smaller, the disparity between etch rates of regions with positive, negative, and zero roughness is reduced, and all regions on the PR surface start laterally etching at almost the same rate. It, therefore, becomes difficult to remove small amplitude roughness and even more difficult small amplitude roughness with low spatial frequency.

To conclude, Figure III-30 shows that using a Cl_2/O_2 trim process limits the pattern reflow and thus the gate shifting, while it leads to improved LWR compared to the reference HBr cure process.

III.3.3.3 Conclusion

In this section we have studied the impact of different chemistries on the resist flowing phenomena and the smoothening of the PR LWR. Two main chemistries have been tested:

- H_2 cure plasma results in an improved LWR due hydrogen radical etching, but lead to a strong flowing due to hydrogen diffusion within the resist bulk.
- Cl_2/O_2 trim step improves the LWR as much as hydrogen steps but without any resist flowing because of the limited VUV flux emission.

At this stage, the best candidates for photoresist pretreatments are either HBr cure steps at low source powers (300w) or Photoresist trim steps in Cl_2/O_2 chemistries.

However, we should still verify that the improved resist patterns obtained after those conditions can be transferred during the subsequent plasma step into the full gate stack.

III.3.4 Gate shifting and LWR transfer after etch

Based on the results obtained in the previous section III.3.3, HBr cure plasma at low source power (300w) or Cl_2/O_2 trim step are the best candidates to improve both the gate shifting and the LWR.

Figure III.33 compares the gate shifting values and the LWR obtained after the standard HBr cure process at 1320 W source power and the improved cure conditions : HBr at 300W and Cl_2/O trim. Figure III.33a clearly demonstrates that with the improved cure conditions, the gate shifting is improved and is comparable to the gate shifting obtained after the lithography of 1nm.

In terms of LWR, HBr cure at 300w as well as trim chemistries present LWR values of 4.1nm and 3.7nm respectively (Figure III.33b), which are lower than the initial LWR after lithography (4.9nm).

However, as explained in Section III.1.2, SiARC etch plasma step can have a strong impact on resist patterns depending if the resist has been cured or not. In Figure III.33, the impact of the Si ARC etching step on the GS and LWR values according to the cure treatment priory applied is also reported. Figure III.34 also shows the pattern profiles obtained after the Si ARC etching process according to the cure treatment used. While this plasma etching step has no impact on the gate shifting (a low GS after treatment will be transferred during the subsequent plasma etching steps whatever the cure treatment used) (cf. Fig III.33a), it can severely degrade the pattern LWR (cf. Figure III.33b).

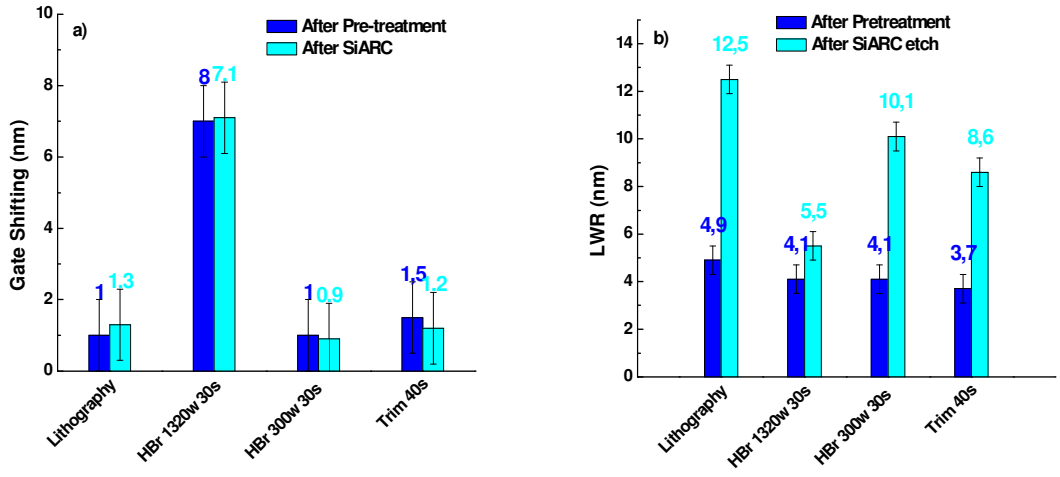

Figure III-33(a) Gate shifting and (b) LWR evolution of lithography patterns after different pretreatment (Lithography, HBr at 1320ws and 300ws and trim in Cl_2/O_2) and exposed to SiARC etch chemistries in CF_4/CH_2F_2.

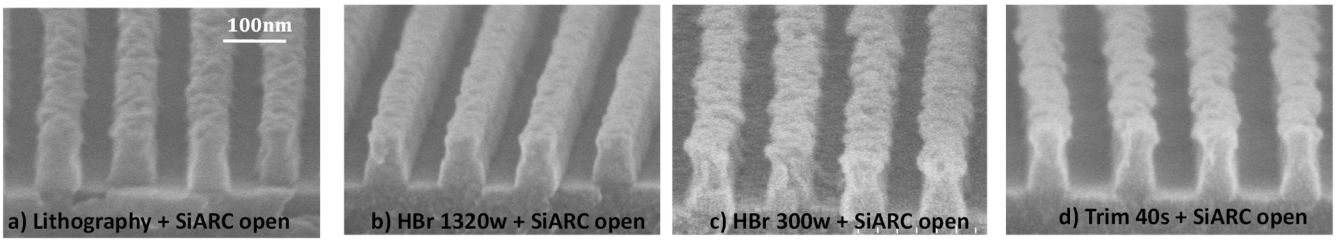

Figure III-34 Cross section images of photoresist and SiARC patterns after (a) Lithography (b) HBr cure at 1320w, (c) HBr cure at 300w, and (d) Trim, in Cl_2/O_2, and exposed to SiARC etch chemistries in CF_4/CH_2F_2.

It can clearly be observed in Figure III.34 that both the top surface and sidewalls roughness are degraded during the Si ARC etching for all cases, although the degradation is much less pronounced if the resist pattern has been cured with the HBr cure treatment at 1320w. Consistently with SEM observations, the LWR values measured after the SiARC etching process are all increased up to around 10nm except in the case of the standard HBr cure process at 1320 W. A roughening mechanism of photoresist films exposed to fluorocarbon plasma chemistries has been proposed in the literature [40]. The synergetic effect of fluorocarbon deposition and ion bombardment during plasma etching in fluorocarbon plasma generates a hard layer on the top surface of the resist film, while the resist bulk remains soft. The stress relaxation of the hard surface layer, generates surface buckling, and then surface roughness. This buckling mechanism is mainly related to the mechanical differences between the stiff surface layer and the underlying soft resist bulk [41]. The magnitude of the stress due to the hard layer and the resulting roughness will change according to the elastic modulus of the soft layer. It is known that the mechanical properties of the photoresist films (or pattern) evolve as a function of the VUV dose received during the treatment. It is believed that for low VUV dose, main chain scission mechanisms occur, softening the resist, while for higher dose cross-linking mechanism and resist densification dominate [42] [12]. Based on these assumptions, it is not surprising to observe in Figures III.33b and III.34 that the resist pattern LWR is much less degraded during the SiARC etching process if previously exposed to HBr cure plasma at 1320W that emits strongly in the VUV range. On the contrary, if the resist is exposed to soft VUV dose, as it is the case for HBr at 300W or trim processes, the resist bulk remains soft compared to the hard fluorocarbon layer, and significant roughness is generated.

In conclusion, although the addition of Cl_2/O_2 trim limits gate shifting, it introduces some LWR issue during the pattern transfer. A more detailed study concerning the pattern transfer will be discussed in Chapter IV.

III.4 Conclusion

HBr Cure has been well established as post-lithography treatments to increase photo-resist stability and to improve LWR and CDU before pattern transfer. However, for the latest 193nm photoresist platforms, this cure step leads to resist flowing that results in the gate shifting phenomenon.

However, if no cure is applied, the gate shifting will be maintained at low value but the photoresist will undergo severe stress during SiARC etching processes and the pattern LWR is degraded during pattern transfer. Therefore, a compromise needs to be found in order to limit both, the gate shifting and the LWR.

While low VUV dose during plasma treatments is required for limiting gate shifting and improving the photoresist LWR, high VUV dose is mandatory to harden the photoresist pattern and prevent from resist LWR degradation during SiARC etching. According to this finding, it means that there is no resist treatment suitable for preserving both the gate shifting and the roughness degradation. At this point some other strategies have to be implemented.

As the gate shifting is the key issue, our choice is, from now on, to apply trim steps only, or, cure treatments with low VUV dose that limit the resist reflow. The consequence is that the SiARC etch step needs to be revisited to improve overall pattern transfer. For this, the mechanisms driving the photoresist roughening effect in fluorocarbon based plasmas need to be understood. Chapter IV will be dedicated to this study in order to propose new SiARC etching process conditions to improve pattern transfer without the use of resist pre-treatments.

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Chapter IV. Photoresist LWR degradation during SiARC etching process and transfer into the gate stack

Chapter III was dedicated to the study of cure pretreatments and their limitations. The HBr plasma post-lithography treatment was identified as being responsible of a local pattern shifting and other candidates such as trim steps have been studied as pre-treatments to improve both resist LWR and gate shifting.

However, preliminary results show that cure step removal reduces the observed pattern shifting but to the detriment of the LWR. Indeed, uncured photoresists lead to unstable resist patterns that undergo severe stress during the subsequent Si-ARC plasma etching (Figure IV-1). Previously shown CD-SEM measurements reveal that state-of-art- CF_4 based plasma chemistries used to etch SiARC layer, strongly increase photoresist surface roughness which is then transferred into the rest of the stack (Chapter III,-section III.3.2).

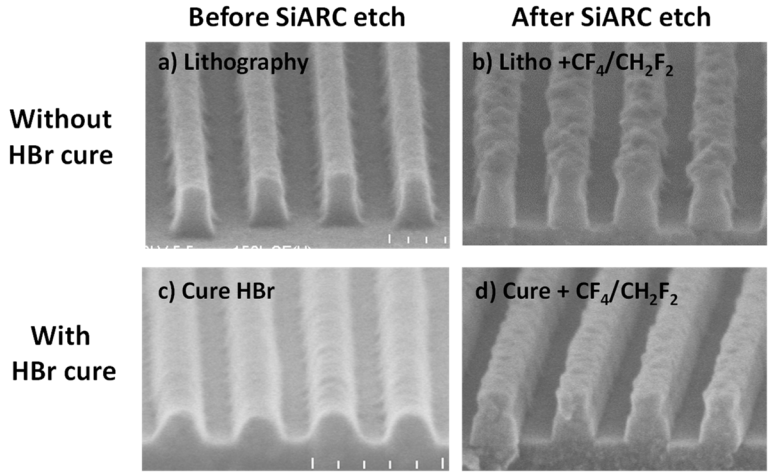

Figure IV-1 SEM cross section images of photoresist patterns (a&c) before and (b&d) after exposure to CF_4/CH_2F_2 SiARC etch process (600V) for reference photoresists (a&b) and photoresists cured in HBr 1320w during 30s (c&d).

In the present chapter, we will further investigate the mechanisms that drive this resist degradation in fluorocarbon based plasmas. Besides, we evaluate how the state of the art gate etch process can be improved, by investigating the impact of each plasma etching steps involved in the high-K metal gate patterning on both LWR and gate shifting.

The chapter will be divided in two main sections. First, we will discuss the impact of the lithography stack etching (Photoresist/SiARC/SoC) where notably the contribution of the SiARC etch step to resist

pattern degradation is studied. Secondly, the LWR transfer into the Hard Mask and gate layers is studied.

IV.1 Impact of SiARC plasma etching process on gate patterning and roughness

IV.1.1 Photoresist degradation in CF_4/CH_2F_2 plasmas

In this section, we will try to understand the mechanisms that lead to photoresist degradation during the pattern transfer in CF_4/CH_2F_2 plasmas. For this, the photoresist roughness evolution during the SiARC etch process is evaluated. Afterwards, photoresist physico-chemical analyses are carried out after exposure to CF_4/CH_2F_2 plasma to analyze the possible material modifications that could be responsible of the degradation and the roughness formation. The initial CF_4/CH_2F_2 process conditions are 600V, RF<500w, P<10mT and an CF_4/CH_2F_2 ratios of (2:1)

IV.1.1.1 LWR/LER degradation during the SiARC etch process

Figure IV-2 shows the roughness evolution of a reference and cured photoresist after exposure to CF_4/CH_2F_2 SiARC etch process. The LWR and LER values are measured from top view CD-SEM images.

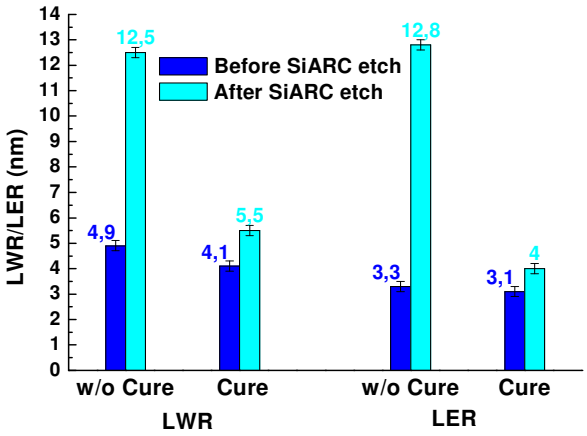

Figure IV-2 Roughness evolution for reference and cured photoresist after exposure to CF_4/CH_2F_2 Si-ARC etch process LWR and LER values were measured from top view CD-SEM images.

As shown in Figure IV-2, the resist LWR/LER are degraded during the SiARC process for both cured and non cured resists, but the degradation is much more significant if no cure is applied prior to the SiARC etch step. For the reference resist, a ~7.5nm LWR increase is measured against only the ~1.5nm observed for the HBr cured resist. For reference photoresist, the LER is more impacted than the LWR, and a LER increase of ~9.5nm was observed. In revenge, the LWR and LER evolution is similar for cured photoresist where only ~1nm LER increase was observed after exposure to CF_4/CH_2F_2 plasmas.

However, as discussed in Chapter II, the CD-SEM metrology is compromised for a precise study of the LER and the roughness transfer mechanism. CD-SEM roughness calculation is carried out from top view SEM images where the sidewall roughness is averaged and LER contributions of PR and SiARC cannot be separated. Besides CD-SEM measurements on photoresist patterns are always questionable because of the impact of the electron beam on photoresist CD and roughness [1]. Thus, for the following studies, the CD-SEM metrology will be only used to provide preliminary LWR and LER information, and to account of the correlation degree between both line edges. For precise roughness analysis, sidewall

AFM metrology will be preferred. This technique allows measuring the roughness variations all over the pattern height and helps us to better understand the roughness evolution along the photoresist and SiARC sidewalls. It should be reminded that the AFM technique only provides LER information and not the LWR.

Thus, AFM technique has been carried out on HBr cured and non-cured photoresist patterns before and after exposure to the SiARC process in CF_4/CH_2F_2. The AFM images obtained after SiARC process in both cases are shown in Figure IV-3. They are consistent with SEM cross section images in Figure IV-1, revealing the very rough top resist surface and the severe sidewalls striations in the case of the non cured resist. From the AFM images, LER can be estimated all along the pattern sidewalls as reported in Figure IV-4. Once the interface between the photoresist and SiARC layer has been determined, an average LER for each material is estimated and is reported on Figure IV-4. The LER is averaged over the whole scanned thickness for each film (SiARC and PR). However, presence of flat surfaces at pattern bottom and also profile rounding at the pattern top sidewall lead to an increased error in the AFM metrology. Therefore, the first and last ~3nm are not considered for the calculation of the averaged LER values (c.f. Chapter II).

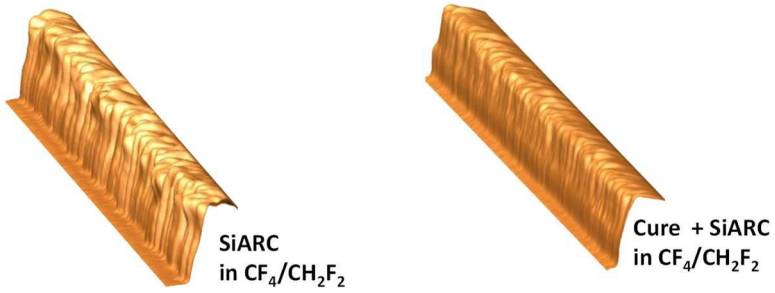

Figure IV-3AFM images of reference and HBr cured Photoresist after exposure to SiARC etch in CF_4/CH_2F_2.

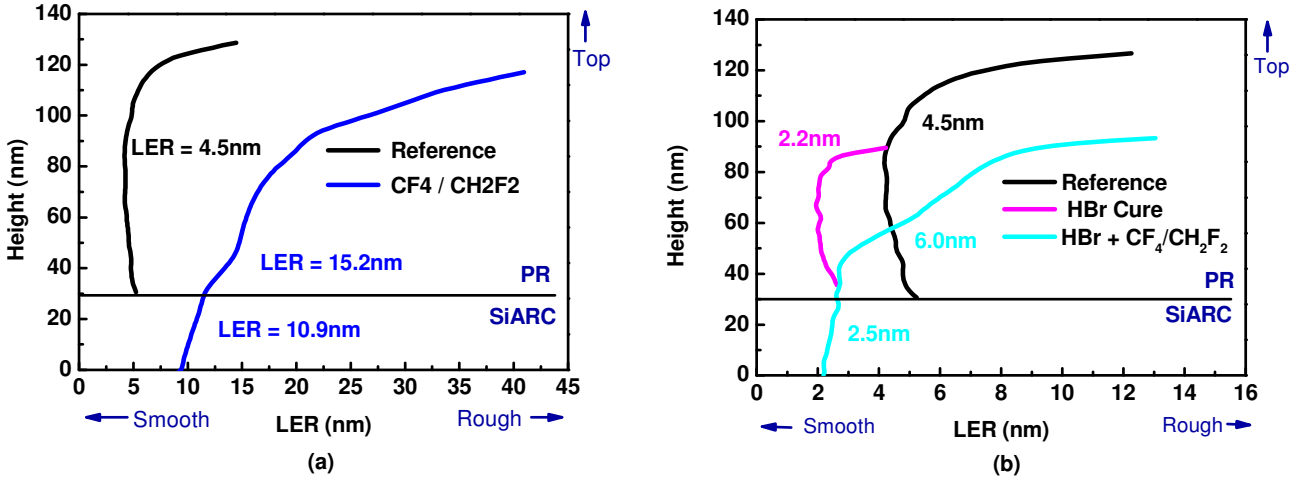

Figure IV-4 LER evolution along the pattern height of (a) reference PR and (b) HBr cured PR after exposure to SiARC etch in CF_4/CH_2F_2. LER values are averaged over the full thickness for each material (PR or SiARC). The first and last ~3nm are not considered for the calculation of the LER averaged values.

Reference photoresist patterns present an averaged LER of ~4.5nm. The AFM measurements show that exposure to fluorocarbon plasma strongly increases photoresist sidewalls roughness (LER 15.2nm), which is much more pronounced at the top than at the bottom of the pattern

In fact, it has been demonstrated in a previous study by *Azarnouche et al* that the LER degradation is a dynamic process [2]. The resist LER starts to be degraded at the top and the degradation propagates along the pattern sidewalls during the SiARC etch process. As long as the degradation has not reached the PR/SiARC interface, the SiARC LER is very close to the initial resist LER value.

Exposure to fluorocarbon plasma strongly increases photoresist surface roughness (LER ~ 15.2nm). The photoresist is generally rougher at the top of the pattern due to the impact of ion bombarding and CF_x deposition. Then, this degradation propagates along the PR sidewalls during the SiARC etch process. The roughness measured at the PR pattern bottom (footing) is the first to be transferred into SiARC. However, the PR roughness evolves during the SiARC etch process and the degradation is partially transferred into the SiARC, leading to final LER values of 10.9nm on the SiARC sidewalls. (Figure IV.4a).

The same trend is observed for cured photoresist patterns (Fig IV-4b). After HBr cure, the LER is decreased down to 2.2nm but during the SiARC etch process, the PR LER is degraded. The LER degradation is more significant at the top of the PR pattern and propagates along the PR and SiARC sidewalls. However, the degradation propagation along the sidewalls is limited compared to the case of reference PR. Consequently, the final LER value measured in SiARC is slightly increased (2.5nm) compared to the initial PR LER after cure (2.2nm), but is considerably lower compared to the reference photoresist where an LER value of 10.9nm is measured.

This lower LER after the SiARC etch process with cured PR is attributed to two contributors. First, the initial lower PR roughness of cured patterns compared to those of reference PR (2.2nm vs 4.9nm). Secondly, several authors [2] [3] have established a direct relationship between surface roughness and line edge roughness in patterned structures. According to their studies, the higher the pattern top surface roughness is, the stronger LER will be obtained. *Engelmann et al* also showed that the polymers with greater plasma induced material loss present increased surface roughness [4] [3] [5]. In other words, for a given plasma condition, polymers with higher vertical etch rate, present a more significant top surface roughness, and therefore a more degraded pattern sidewall LER.

Figure IV-5 shows that cured resists are etched less rapidly than reference resists during the SiARC etch process in CF_4/CH_2F_2. This could be explained by the resist densification induced by the strong VUV irradiation of HBr plasma treatment, as explained in Chapter III. Consequently, for the same SiARC processing time, the amount of removed PR material during the SiARC process is lower in the case of cured resist than of reference resists, resulting in lower surface roughness.

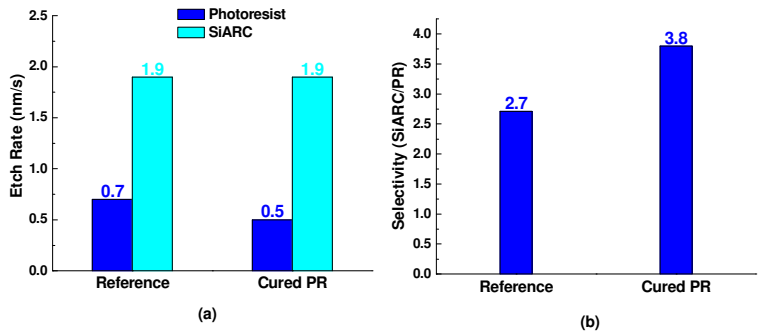

Figure IV-5(a) Etch rates and (b) selectivity of photoresist (reference and HBr cured) and SiARC layers after exposure to SiARC etch conditions in CF_4/CH_2F_2plasma.

In conclusion, when exposed to SiARC etch conditions in CF_4/CH_2F_2 the photoresist top surface is degraded. The top surface degradation propagates through the pattern sidewall from the top to the bottom of the pattern and is partially transferred into SiARC, leading to increased LER and LWR. Addition of cure steps before SiARC etching limits the top surface degradation and thus the LER increase.

However, as explained in Chapter III, cure step integration leads also to Gate Shifting. Our aim is to avoid the GS phenomenon; therefore, it is mandatory to remove the cure step. Consequently, the photoresist surface degradation mechanisms during SiARC etching in CF_4/CH_2F_2 need to be better understood in order to be avoided.

IV.1.1.2 Origin of the photoresist degradation in Fluorocarbon chemistries

In this section, the impact of the SiARC etch process conditions on the photoresist degradation is studied. For this, we preferred working on reference photoresist patterns without any cure to avoid the gate shifting phenomena. According to the literature, polymer degradation upon exposure to fluorocarbon chemistries strongly depends on the energy density deposited on the photoresist surface [4]. Therefore, to study the evolution of the PR sidewall roughness with process conditions, PR patterns were exposed to CF_4/CH_2F_2 plasmas with different applied bias voltages (from 70 to 600V). Note that in the standard process conditions the SiARC etch is carried out at 600V.

a) Roughness evolution with ion energy

Figure IV-6 shows SEM cross section images of PR/SiARC stacks etched in CF_4/CH_2F_2 plasmas with different ion energies.

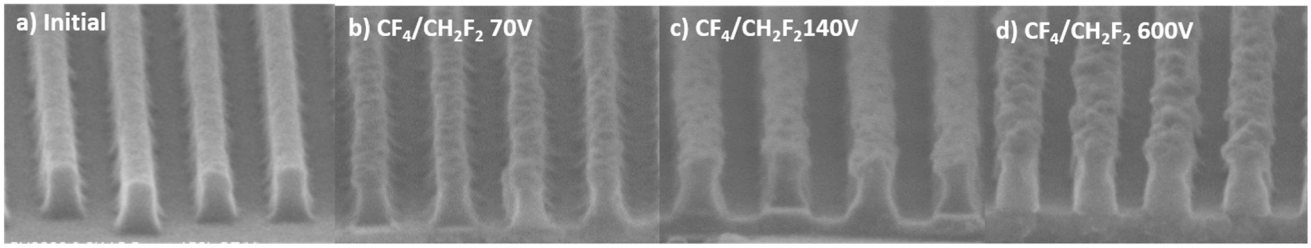

Figure IV-6 SEM Cross section images of photoresist patterns (a) after lithography and exposed to CF_4/CH_2F_2 plasmas at (b) 70V (c) 140V and (d) 600V applied bias (standard conditions). Other plasma parameters remain the same for both conditions

From Figure IV-6, it seems that the photoresist top surface degradation can be decreased with decreasing applied bias voltage. However, it is also clearly observed that decreasing applied bias voltage is detrimental to the SiARC profile, and then to the CD control. At 600V the SiARC profile is straight; while tapered profile with a strong footing is observed at 70V, typically attributed to strongly polymerizing etch processes.

To confirm the resist degradation with ion energy bombardment, AFM analyses are carried out on photoresist blanket films exposed to CF_4/CH_2F_2 plasmas with different applied bias voltages (70V, 140V and 600V) during 10s (Figure IV-7). In fact, we can consider that the degradations observed on blanket PR wafers are representative to the degradations occurring at the top of the PR patterns. The obtained AFM measurements are consistent with the SEM observations and confirm an increase of the photoresist surface roughness with ion energy.

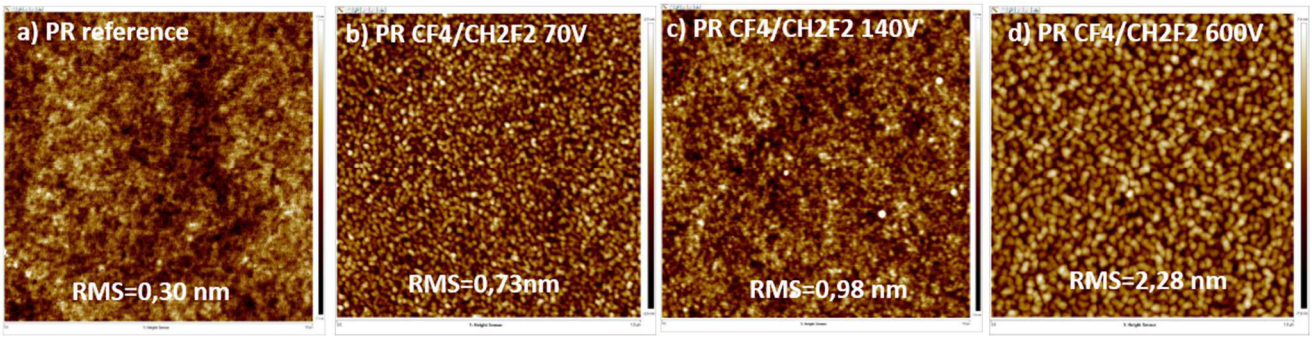

Figure IV-7 AFM images of photoresist layers (a) as deposited and exposed to a CF_4/CH_2F_2 plasmas with(b) 70V (c) 140V and (d) 600V applied bias voltages (std condition).

The sidewall roughness evolution with applied voltage is also measured by top view CD-SEM and is shown in Figure IV-8.

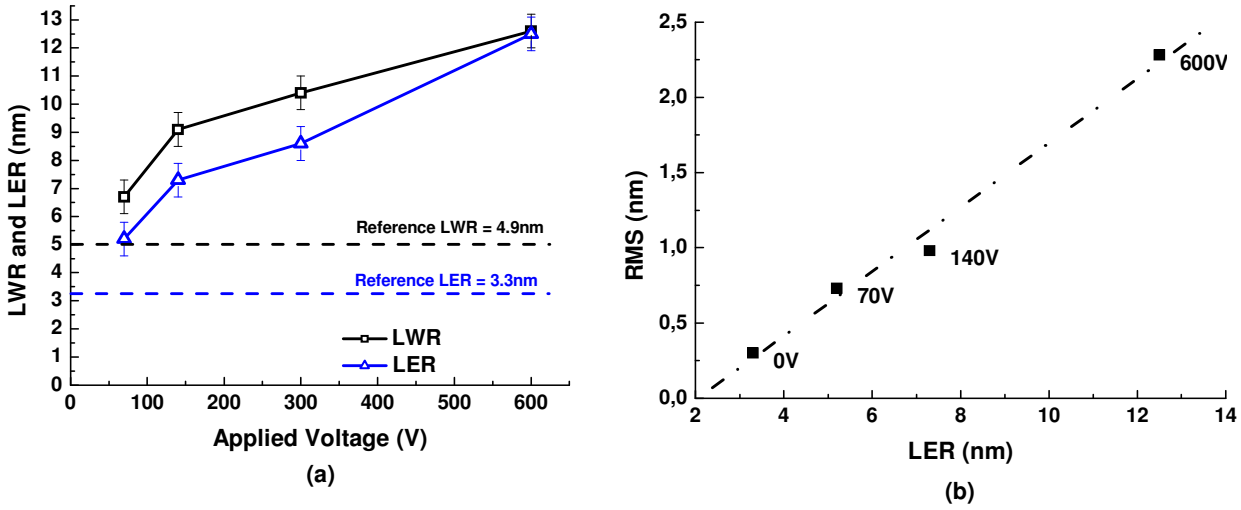

Figure IV-8(a) Roughness (LWR &LER) evolution with the applied bias voltage. LER and LWR are measured from top view CD-SEM images. (b) RMS roughness as a function of the LER for a Photoresist exposed to CF_4/CH_2F_2 plasmas for different bias voltages.

A continuous increase of the LWR and LER is observed with increasing bias voltage, due to the increase of PR sputtering (Fig IV-8a) and Fig IV-8b suggests that, this increase is directly correlated to the increase of the top resist surface roughness with applied bias. This result is in a good agreement with previous studies [2] [3]and confirms that the degradation of the photoresist top surface roughness is directly responsible for the sidewalls roughness increase during plasma exposure.

Although the photoresist surface degradation can be reduced by limiting the ion sputtering in CF_4/CH_2F_2, low ion energy bombardment is not recommended to etch the SiARC layer with a good anisotropy and CD control.

In the next section we propose to bring some understanding of the mechanisms involved in the photoresist surface roughening with bias voltage in CF_4/CH_2F_2 plasma conditions.

b) Photoresist and SiARC etch rates

To compare the SiARC and PR etch mechanisms in CF_4/CH_2F_2 based plasmas, both material ER was measured as a function of the applied voltage. *Steinbrüchel et al* [6] proposed a universal equation to describe all types of ion bombardment-induced etch processes such as physical sputtering or ion-enhanced chemical etching. This method consists in tracing the material etch yield as a function of the ion energy square root:

$$EY = A\,(E_i^{1/2} - E_{th}^{1/2}) \qquad \text{(Eq. IV.1)}$$

Where, *EY* is the etch yield, *A* is a constant dependent of the target material, E_i is the ion energy ($E_i = V_P - V_{DC}$, considering V_P, a plasma potential of ~15V and V_{DC} the applied bias voltage) and E_{th} is the energy threshold required for the reaction to occur.

The ion induced etch rate (ER) is related to the etch yield (EY) by the following formula [4]:

$$ER = v_i EY \Gamma_i \qquad \text{(Eq. IV.2)}$$

Where, v_i is the substrate volume removed per impacting ion and Γ_i is the ion flux. However, since our experiments are carried out in an industrial based etch reactor, we could not measure the ion flux, and therefore, we could not estimate the etch yield per unit volume. However, assuming that the ion flux does not change significantly with E_i, the ER should be proportional to EY and therefore to the $\sqrt{E_i}$ [7]. According to this assumption, we have then plotted the PR and SiARC etch rates (ER) as a function of the ion energy square root ($\sqrt{E_i}$):

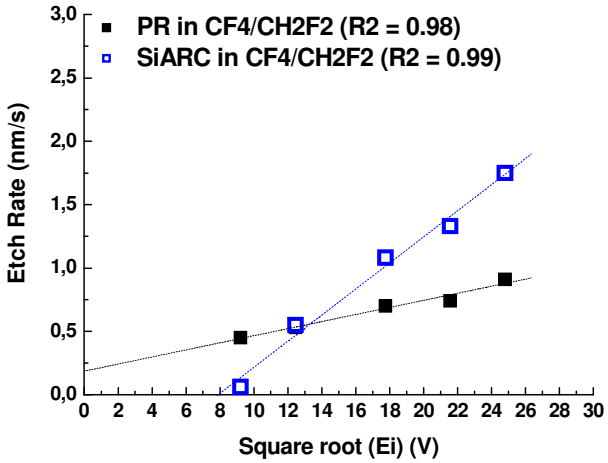

Figure IV-9PR and SiARC etch yield in CF_4/CH_2F_2 plasma as a function of the square root of incident ion energy. The dashed lines represent the linear fit of the obtained data.

The SiARC ER shows a linear dependence with the square root of the ion energy, with an ion energy threshold of about 64eV. At low bias voltages, no SiARC etch will occur, resulting in a bad PR/SiARC selectivity. In revenge, at high bias, the SiARC follows and ion-enhanced etching mechanism and the SiARC ER will increase with ion energy. This result agrees with previous studies carried out by *Karahashi et al*, where SiO_2 films were sputtered by fluorocarbon ions CF_x (X = 1,2,3) [8]. According to their work, at high ion energies the SiO_2 etching yield increases with increasing ion energy while at low

ion energies, no steady state etching occurs and a a-C:F film is deposited on the SiARC surface stopping the etching [9] [8].

However, for the photoresist, no energy threshold is observed and the PR etch rate is very low and almost constant with ion energy. In CF_4/CH_2F_2 plasma conditions, the photoresist etch rate is not limited by the ion energy, but rather by a lack of reactive species (i.e. fluorine) bombarding the polymer surface.

In conclusion, from the ER analysis as a function of the applied bias voltage we can assume that:

- **The SiARC etch rate is limited by ion energy and at low ion energies FC film deposits over SiARC stopping the etch process**
- **The PR etch rate is not dependent on ion energy but is limited by the available reactive species (i.e. Fluorine)**

c) Surface analysis by XPS

- **Experimental Protocol**

To confirm the assumptions done concerning the etch mechanism of SiARC and PR in CF_4/CH_2F_2 angle resolved XPS (AR-XPS) analyses are carried out. To simulate real patterning conditions with about 50%-50% of PR-SiARC open areas, and avoid macro-loading effects between full-sheet and patterned wafers, 70nm thick SiARC samples (representing half of the total wafer area) are patched over 100nm thick PR blanket wafers as described in Figure IV-10.

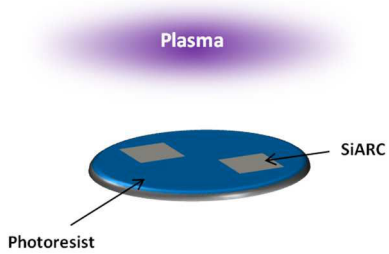

Figure IV-10 Schematic representation of the experimental protocol used for AR-XPS sample elaboration

The wafers are then exposed to SiARC etch process conditions in CF_4/CH_2F_2 during 10s. Both, SiARC and PR surfaces present on the wafer are then characterized by AR-XPS. Two bias voltage conditions have been investigated 70V and 600V (standard condition). For all samples, peaks were fitted considering the peak shift of C-C and C-H bonds at 285eV. For further experimental detail, refer to Chapter II. For clarity, the surface analyzed at θ = 76º will be considered "extreme surface" and the surface at θ = 23º will be considered as "bulk" for the rest of this chapter.

- **XPS analysis on SiARC surface**

Figure IV-11 shows the C1s, O1s Si2p spectra (taken at θ = 76º) of a SiARC sample before and after exposure to a CF_4/CH_2F_2 plasmas using either 70V or 600V bias voltages. The binding energies of the relevant peaks are also listed in Table IV-1 and Table IV-2.

Tableau IV-1 Binding energy (eV) and Atomic contribution (%) of the main elements composing the extreme surface (θ = 76) of a SiARC sample exposed do CF_4/CH_2F_2 plasmas.

Atomic composition (%)															
	C1*s*							O1*s*			Si2p			F1s	
Bonding	C-C. C-H	C-CF	C-O-C	C-F	C=O	C-F2	CF3	SiO-C	O-Si	SiO-F	C-SiO	Si-O	F-SiO	F-Si	F-C
Binding Energy (eV)	285.0	286.3	287.0	288.2	289.0	290.4	292.9	532.2	533.2	533.7	102	103.4	104	687.7	688.8
Reference (At%)	26.2	-	1.4	-	-	-	-	6.9	41	-	2.7	21.7	-	-	-
After FC 70V (At %)	4.2	9.8	-	10.2	-	8.8	1.8	3.4	8.8	2.1	2.2	1.9	3.0	10.0	33.8
After FC 600V (At%)	7.8	10.1	-	6.3	-	2.9	0.4	3.1	16.0	8.8	2.2	10.3	4.1	11.8	16.1

Tableau IV-2 Summary of each element's total atomic contribution (%) at (θ = 76)

Elements	C1s	O1s	Si2p	F1s
Reference SiARC (At%)	27.4	47.9	24.4	-
After FC 70V (At %)	34.8	14.3	7.1	43.8
After FC 600V (At %)	26.9	27.9	16.6	27.9

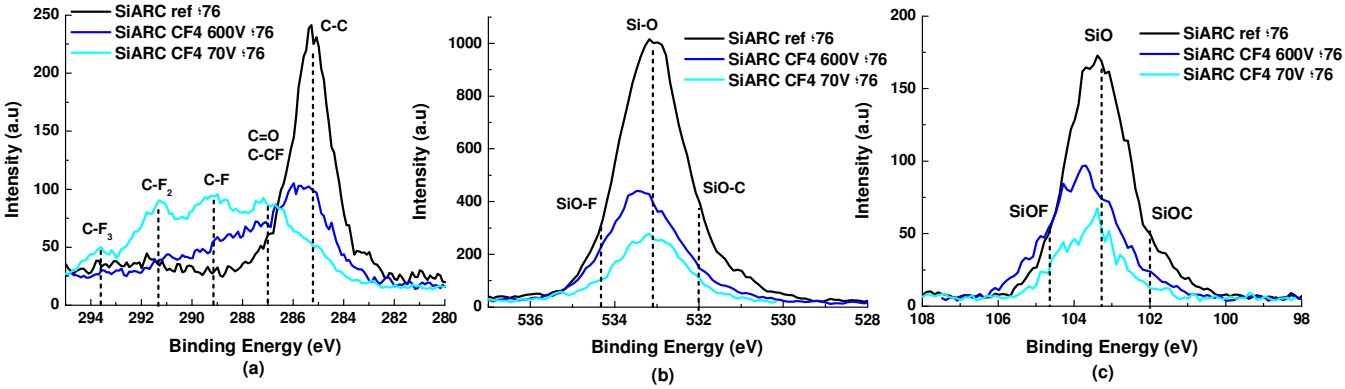

Figure IV-11 (a) C1s (b) O1s and (c) Si2p spectra of a SiARC sample as received and exposed to a CF_4/CH_2F_2 plasma at 70 and 600V. Spectra were taken with an AR-XPS at θ=76° to analyze the contribution of the surface reactive layer. Peaks were shifted according to the C-C or C-H peak at 285eV.

The non-exposed SiARC C1s spectra only present one carbon contribution at 285eV coming from the C-C and C-H bonds of SiOCH (Fig IV-11a). However, under plasma exposure, the C-H contribution is strongly reduced and the presence of several peaks between 285eV and 293eV is observed attributed to the presence of fluorocarbon species **[10]**. The peak at 286.2eV is assigned to C-CF_x species while the three other peaks are associated to carbon bonded to fluorine at different fluorination states: C-F at 288.2eV, CF_2 at 290.1eV and CF_3 at 292.8eV (cf. Table IV-1).

The O1s and Si2p spectra are fitted considering three oxygen contributions, identified as the Si-O, Si-O-C and Si-O-F bonds. The reference SiARC silicon and oxygen compositions are similar to those of silicon oxides, with a main O1s contribution at 533eV (Fig. IV11b) and a Si2p contribution at 103.3eV (Fig. IV-11c) attributed to the Si-O bonding. A smaller contribution is observed at 532eV for the O1s peak and at 102eV for the Si2p peak attributed to respectively the O-C and Si-O-C binding energies. After plasma exposure, the O1s and Si2p peaks are shifted towards higher binding energies. This shift is attributed to SiARC surface fluorination by the formation of F-Si-O bonds appearing in O1s and Si2p peaks at 534eV and 104eV respectively.

The evolution of the main elements of the SiARC composition as a function of the analyzed angle is shown in Figure IV-12 for reference SiARC and samples exposed to fluorocarbon plasma at 70V and 600V (standard condition). It should be considered that information obtained at a θ = 76° corresponds to first 1-2nm while the data at θ = 23° correspond to a maximum proved thickness of 6-9nm. [5]

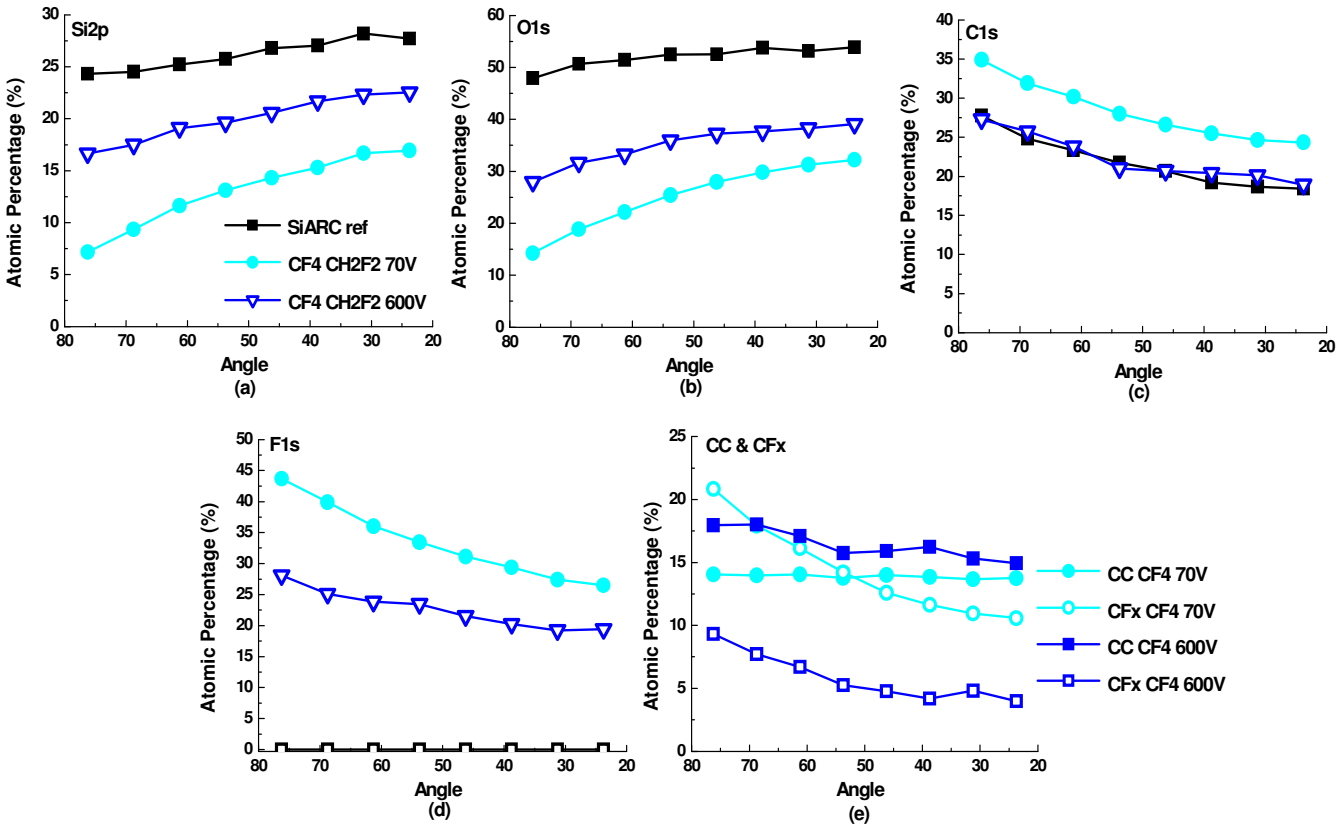

Figure IV-12. Evolution of the SiARC elemental composition as a function of the analyzed angle for SiARC samples before and after exposure to CF_4/CH_2F_2 plasma at 70V and 600V: a) Si2p; b) O1s; c) C1s, d) F1s and e) CC and CFx contributions. The C-C and C-CFx contributions have been gathered under the label "C-C", while CF, CF_2 and CF_3 contributions are represented by the label CF_x.

As observed in Fig IV-12, after FC plasma exposure, there is a general loss of the oxygen and silicon content which is partially due to a fluorination of the surface. The loss is more pronounced at the extreme surface and more important in the case of 70V compared to 600V. Besides, at 70V, the SiARC layer is clearly enriched in carbon within the whole probed thickness while no change in the total carbon content is observed for samples at 600V compared to the reference. A more detailed analysis of the carbon composition is given in Fig. 12e where the C-C and C-CF_x contributions have been gathered under the label "C-C", while CF, CF_2 and CF_3 contributions are gathered and represented as "CF_x" layers. At 600V, the "CC" contribution is more important than the "CF_x" one for all the probed depth. On the contrary, at 70V, there is a significant CFx contribution at the extreme surface that decreases with the probed thickness while the CC contribution is almost constant all over the probed thickness. This preliminary analysis indicates that at 70V there is the formation of a CF_x deposition on the Si ARC surface, while at 600V there is a fluorination of the SiARC surface which is more pronounced at the extreme surface. To go further with the analysis, the Si/O, Si/CC and F/C ratios have been plotted as a

function of the angle of analyze. Considering silicon coming only from the SiARC substrate, the Si/O ratio is measured by dividing the Si2p total contribution by the O1s total contribution.

The Si/C and F/C ratios are calculated by the Equations 3 and 4 given below. By this, for the Si/C ratio, we consider only the SiARC carbon composition to determine if the Si-O-C bond coming from substrate is being etched. The carbon addition due to plasma induced polymer deposition is therefore not considered. For the F/C only the fluorine forming F-C bonds is considered, so that we can determine the nature of the CF_x layer.

$$\frac{Si}{CC} = \frac{Si2p}{(CC+CCF)_{C1s}} \qquad \text{(Eq. IV.3)}$$

$$\frac{F}{C} = \frac{(3\cdot CF3+2\cdot CF2+CF)}{Ctot} \qquad \text{(Eq. IV.4)}$$

Where *CF3, CF2* and *CF* are the atomic percentage contribution of the C-F_3, C-F_2 and C-F bonds measured from the C1s peak, and C_{Tot} is the total C1s carbon contribution.

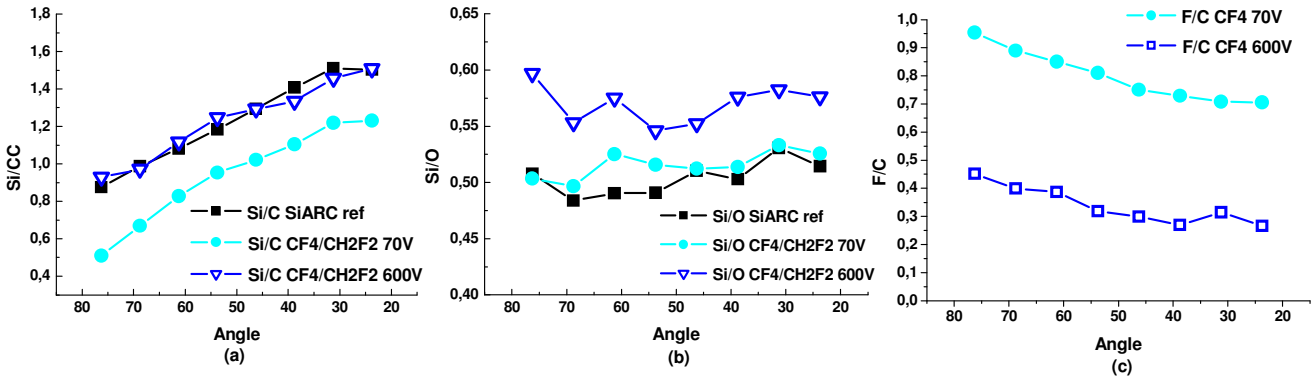

Figure IV-13 (a) Si/CC (b) Si2p/O1ss and (c) F1s/C1s ratio evolution with scanning angle for an SiARC layer before and after exposure to a CF_4/CH_2F_2 plasma at 70V and 600V. θ = 76º refers to extreme surface while θ = 23º is relative to SiARC bulk. The Si/CC and F/C ratios are calculated following equations 3 and 4

As observed in Fig. IV-13, at 70V, the Si/CC ratio is lower than the reference for any proved angle which is probably attributed to the screening of the Si contribution due to a strong CF_x deposition at low bias voltages. This FC film appears to be quite rich in fluorine, particularly at the extreme surface (fig 13 IV-c). In addition, the Si/O ratio does not seem to be strongly modified which suggests that there is no preferential etching of silicon or oxygen. These results confirm the formation of CF_x polymer deposition on the SiARC surface at 70V, which blocks the SiARC etching. This assumption is consistent with the very low SiARC etch rate obtained at 70V.

At 600V, the Si/O ratio is increased compared to the reference for any probed angle, while the Si/CC remains unchanged. This suggests that the SiARC layer has been depleted in O certainly by a fluorination of the surface where O-Si-O bonds are replaced by F-Si-O bonds. The Si/O and F/C ratios are quite uniform all over the surface, which suggests that the reactive layer is quite homogeneous over the entire probed surface. It should be noted that at 600V, the F/C ratio is lower than at 70V, probably due to ion induced fluorine depletion of the FC film **[10]**. These results suggest that at 600V there is a formation of a mixed reactive layer composed of SiOFC (depleted in Oxygen) and CF_x. The SiARC etching in CF_4/CH_2F_2 proceeds through a FC deposition that provides fluorine to form SiF_4 volatile compounds

[11]and carbon to contribute to the SiARC oxygen depletion by formation of CO, CO_2 and COF volatile compounds [11]. **Ion bombardment, certainly by CF_x species, contributes to Si-O bond breaking and results in a preferential oxygen removal and the replacement of Si-O bonds by Si-F bonds. If the ion bombardment becomes too low (i.e. 70V), the CF_x cumulate forming a FC layer that prevents ion penetration and blocks the SiARC etching [12]. In revenge, at high ion energies (i.e. 600V), the CF_x bombardment enhances the CF_x implantation and fluorine diffusion by ion induced interface mixing [10]**.This ion mixing results in a uniform reactive layer composed of carbon, oxygen, fluorine and silicon that is responsible of the SiARC etching. [10]

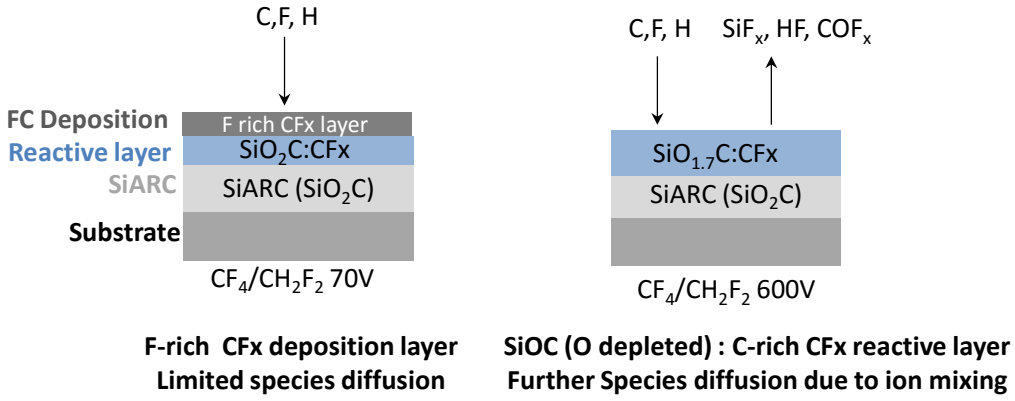

Figure IV-14 Schematic representation of the SiARC surface in CF_4/CH_2F_2 at 70V and 600V

In conclusion, the SiARC etch rate is limited by two components [12] [13] [14]:

- **Diffusion of reactive species (i.e. F and C) towards the SiARC surface**
- **The energy required to ensure chemical reaction and byproduct desorption**

Thus, in CF_4/CH_2F_2 plasmas at 70V, the etch rate is limited by ion energy, while at 600V, the SiARC etch rate is limited by the supply in reactive species.

- **XPS analysis on Photoresist surface**

The XPS spectra taken with a collection angle of 76°, obtained before and after photoresist exposure to CF_4/CH_2F_2 plasmas at 70V and 600V (standard condition) are shown in Figure IV-15. The atomic composition of the surfaces extracted from the peak fitting procedure is detailed in Tables IV- 3 and 4.

Tableau IV-3 Binding energy (eV) and Atomic composition (%) of the main elements composing the extreme surface reactive layer (θ = 76) of a PR sample exposed do CF_4/CH_2F_2 plasmas at 70V and 600V*

	C1*s*							O1*s*			F1*s*		
Bonding	C-C. C-H	C-CF	C-O-C	C-F	C=O	C-F2	CF3	O=C	O-C	O-C-F	F-C (F poor)	F-C	F-C (F rich)
Binding Energy (eV)	285.0	286.3	287.0	288.2	289.0	290.4	292.9	532.2	533	533.7	687	688	688.8
Reference	44.3	-	10.6	-	12.2	-	-	13.3	10.7	-	-	7.6	-
After FC 70V	10.6	12.9	-	13.7	-	10.1	2.2	-	1.6	2.2	-	31.8	14.5
After FC 600V	27.5	16.2	-	12.4	-	7.5	2.1	-	2.5	2.4	24.5	4.9	-

*Note that for all PR samples, 0.5-1% of Sulfur is observed (S2p) which will not be considered in this analysis

Tableau IV-4 Summary of each element's total atomic contribution at (θ = 76)

Element	C1s	O1s	F1s
Reference PR	67,1	24	7,6
After FC 70V	49,5	3,8	46,3
After FC 600V	65,7	4,9	29,4

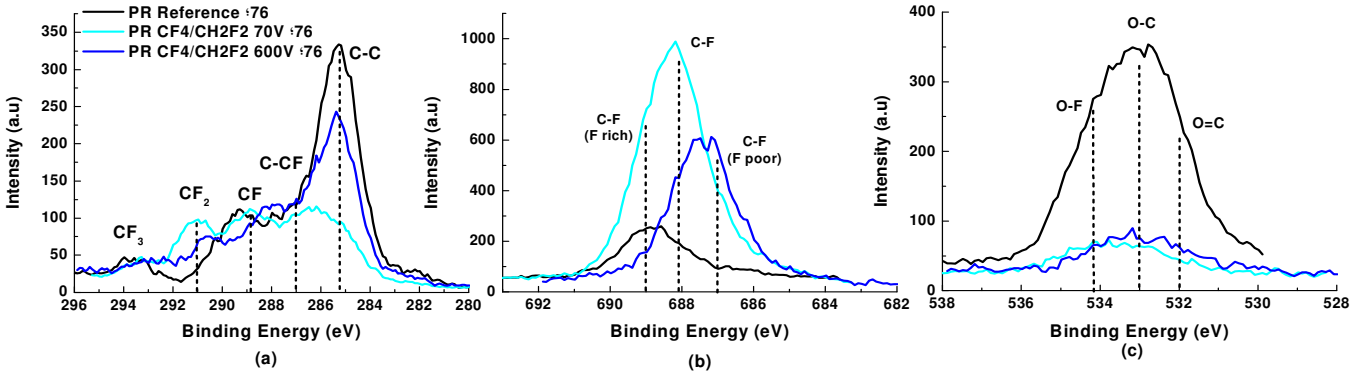

Figure IV-15(a) C1s (b) O1s and (c) F1s spectra of a photoresist B before and after exposure to CF_4/CH_2F_2 plasma at 70 and 600V. Spectra were taken with an AR-XPS at θ=76° to analyze the contribution of the surface reactive layer. Peaks were shifted according to the C-C or C-H peak at 285eV.

In Figure IV-15a, the C1s contribution of a photoresist exposed to fluorocarbon plasma (at 70V and 600V) is compared to the non-exposed photoresist. The pristine resist has a main peak at 285eV attributed to C-C and C-H bonds of the polymer matrix. Lower contribution of lactones and ester C=O peaks at 287.3eV and C-O-C peak at 289.3eV are also observed. The contribution at 294eV is typically attributed to the CF_3 groups coming from the remaining PAG molecules within the film. After plasma exposure, the C1s spectra is deconvoluted with 5 peaks corresponding to the formation of CF_x species (cf. Table IV-4): CC at 285eV, CCF_x at 286eV, C-F at 288.2eV, CF_2 at 290.1eV and CF_3 at 292.8eV (cf. Table IV-1).

The F1s spectra is fitted considering two F-C contributions for each sample whose position may vary depending on the carbon fluorination state, CF_x (X = 1, 2, 3). Thus the reference PR presents an F-C peak at 688.8eV attributed to the CF_3 groups linked to the remaining PAG or to surface free fluorine contamination.

The O1s spectra is fitted considering three oxygen contributions, the O=C at 532eV and O-C bonds at 533eV attributed to PR lactone and ester groups and a contribution at 533.8-534eV which can be attributed either to O-C-F products or to O-H bonds due to H_2O adsorption on the PR surface. Due to sample contamination, this contribution at 533.8eV is already present in pristine PR.

For a further description of the whole probed thickness composition, the evolution of the photoresist elemental composition as a function of the analyzed angle is also shown in Figure IV-16.

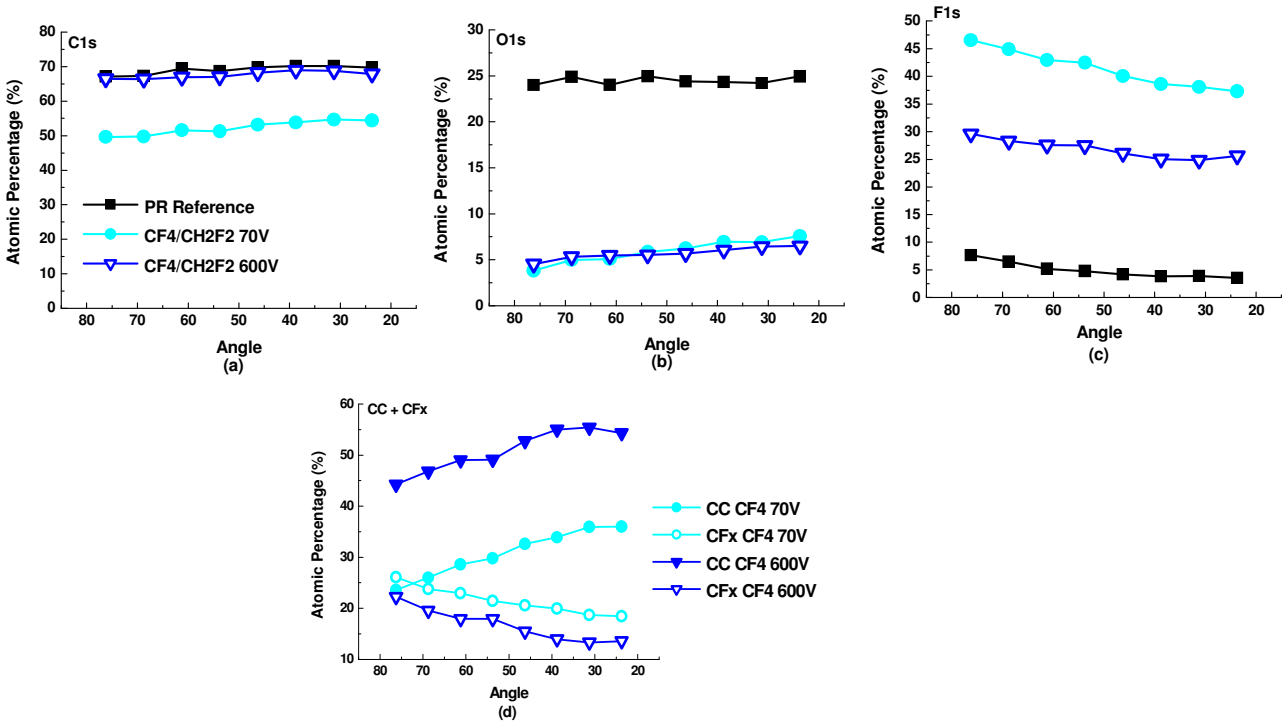

Figure IV-16. Evolution of the elemental composition as a function of the analyzed angle for photoresist before and after exposure to CF_4/CH_2F_2 plasma at 70V and 600V: a) C1s; b) O1s; c) F1; d) CC and CFx contributions. The C-C and C-CFx contributions have been gathered under the label "C-C", while CF CF_2 and CF_3 contributions are represented by the label CFx.

The reference resist is homogeneous in composition on all the probed thickness (70% of C and 24% of O, with some traces of fluorine (6%). Note that H contributions are not detected by XPS.

After plasma exposure at 600V, the atomic composition of the probed surface is almost constant over the whole proved depth (about ~67% of C, ~30% of F, and ~5% of O for all angles). The surface is depleted in Oxygen compared to the reference in favor of fluorine incorporation, the carbon content being similar to the reference. The fluorine concentration is slightly higher at the extreme surface and forms a CF_x reactive layer (cf. Figure IV-16d). The XPS data suggests that at 600V, most of the oxygen present in the film has been replaced by fluorine atoms to form a CF_x reactive layer slightly richer in CF_x at the extreme surface

After plasma exposure at 70V, there is an oxygen and carbon depletion and a strong fluorination of the surface especially at the extreme surface. The surface's carbon environment varies with depth, and presents a greater amount of CF_x and F contributions at the extreme surface in detriment of CC contributions (cf. Figure IV-16d). In this case, it is suspected that there is formation of a CFx deposition at the extreme surface that screens the C1s and O1s signal that accentuates the O1s and C1s depletion compared to the 600V case. To determine the fluorination degree of a polymer surface typically we refer to the F/C ratio. This ratio is determined considering only the fluorine bonded to carbon by using the Equation 4 described in the previous section (referred as F/C in this work). The obtained results are shown in Figure IV-17.

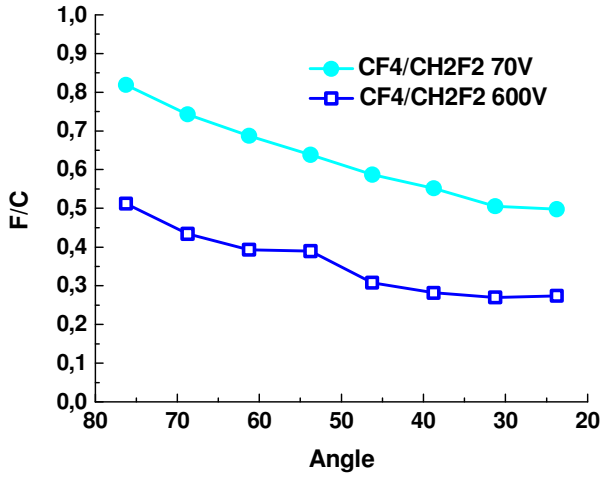

Figure IV-17 F/C ratio evolution with analyzed angle determined using Equation 4. F/C considers only the fluorine that bonded to carbon forming an F-C bond.

According to Figure IV.17, within the whole scanned thickness, the F/C ratio measured over PR films exposed to CF_4/CH_2F_2 at 70V is richer in fluorine than that obtained at 600V.

This suggests that, at low ion energy (i.e. 70V), the plasma supplies enough reactive species to form CF_x surface layer rich in fluorine. In this condition, the etching is limited by the desorption of the etch byproducts due to low ion bombardment. Increasing the ion energy (i.e. 600V) leads to the sputtering of the surface fluorine and the CF_x layer. The surface is therefore depleted in fluorine and presents a more carbon like structure than CF_x like, which explains the significant amount of C1s peak at 285eV in Figure IV15a. In this case, the PR etch rate is higher than that at 70V due to ion induced sputtering but it is limited by the supply in reactive species such as fluorine.

d) Conclusion

From these results we conclude that the same plasma (CF_4/CH_2F_2) behaves differently on SiARC and resist materials with increasing bias voltage.

At low bias voltages, FC deposition occurs on SiARC. This fluorocarbon layer contributes to the ion energy dissipation **[10]** **[12]**and therefore blocks the SiARC etching process. In revenge, at low bias voltages, the Photoresist is actually etched because a fluorine rich CF_x reactive layer is formed on the PR surface that provides enough fluorine for resist chemical etching. The difference in the SiARC and PR etch rates at low bias voltages results in tapered SiARC profiles and etch stop while the PR is laterally etched (Figure IV-6b). Concerning the LWR, previous studies propose that the stress relaxation of the hard FC layer onto the soft PR bulk, generates surface buckling, and promote surface roughness **[15]**. In the case of a PR exposed to a CF_4/CH_2F_2 at 70V, this buckling mechanisms could explain the PR roughness increase observed at 70V in Figure IV- 8 (a & b).

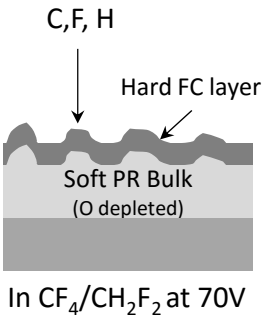

Figure IV-18 Schematic representation of the buckling mechanism of PR in CF_4/CH_2F_2 plasmas at 70V

When the applied bias voltage is increased, the SiARC follows an ion enhanced chemical etching mechanism and its etch rate is increased which results in the formation of straight SiARC profiles (Figure IV-6d). Concerning the photoresist, the increased ion energy contributes to the PR surface fluorine depletion and CF_x sputtering and results in the formation a carbon like surface layer [5] [3]. Due to the inhomogeneous sputtering of the CF_x layer, the FC distribution will not uniform over the whole PR surface. Therefore, the differences in the sputtering efficiency of the remaining hard FC layers and soft PR bulk result in PR micro-masking that strongly degrades the PR surface top roughness, and consequently, the sidewalls roughness [16] [17]. This micro-masking effect explains the LWR increase observed at 600V in Figure IV-8 (a & b).

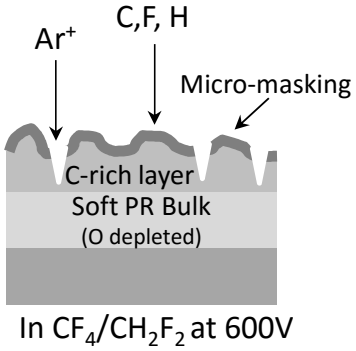

Figure IV-19 Schematic representation of the roughness generation due to PR micro-masking in CF_4/CH_2F_2 at 600V

So, in conclusion, the photoresist degradation results from the synergy of the formation of FC reactive layers that induces buckling and strong ion bombardment that enhances PR micro-masking. It should be noted that, when no fluorocarbon is present, for example, in pure Ar plasmas the photoresist is degraded only due to ion bombardment (no micro-masking), and therefore, the observed LWR values are lower to those measured over photoresists exposed to fluorocarbon based plasma conditions (Fig. 20).

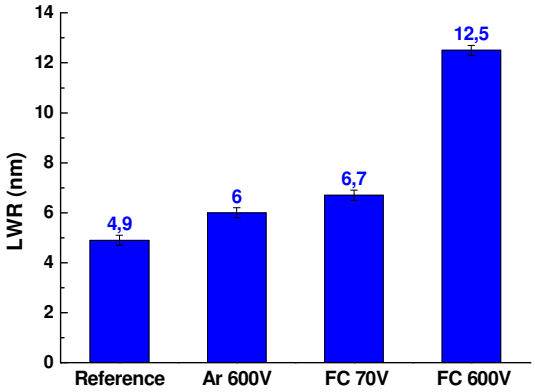

Figure IV-20 LWR values measured over PR patterns after lithography, and after exposure to plasma conditions in Ar at 600V and CF_4/CH_2F_2 at 70V and 600V.

Ideally, working at low ion energies is required to limit the PR degradation. However, this strategy impacts the SiARC etching process which is not etched at low bias voltages and will lead to tapered SiARC profiles. **It seems difficult to find a good compromise between a suitable SiARC etching process and a limited PR degradation in CF_4/CH_2F_2 based plasmas.**

Several tests were carried out tuning the CF_4/CH_2F_2process conditions (Source power, Pressure, Ratio…) to search for an optimum process condition (See Annex II). However, despite the many efforts done, any process carried out in CF_4/CH_2F_2 based plasmas led to a strong PR degradation and strong roughness values which do not satisfy our patterning requirements. **Chemistries richer in fluorine and with soft plasma conditions are then required.**

IV.1.2 SF_6/CH_2F_2 plasma chemistries for SiARC etching

To limit photoresist degradation, fluorine rich plasma processes with low ion energy are required. SF_6/CH_2F_2 gas mixtures have been well reported as plasmas for silicon etching **[18]** and are known to etch SiO_2 efficiently. In this study, we propose to test the ability of the $SF_6/N_2/CH_2F_2$ plasma developed to etch the polysilicon gate to etch the SiARC layer. Initially, due to the high ER reported in SF_6, soft plasma conditions were chosen: 70V, RF<500w, P<10mT and $SF_6/N_2/CH_2F_2$ ratios of (1:1.5:1.5).

IV.1.2.1 Process Results

a) Pattern profiles

Figure IV-21 shows SEM cross section images of the photoresist and SiARC profiles obtained after SiARC etching using either the standard condition in CF_4/CH_2F_2 (at 600V) or SF_6/CH_2F_2 (at 70V) plasma.

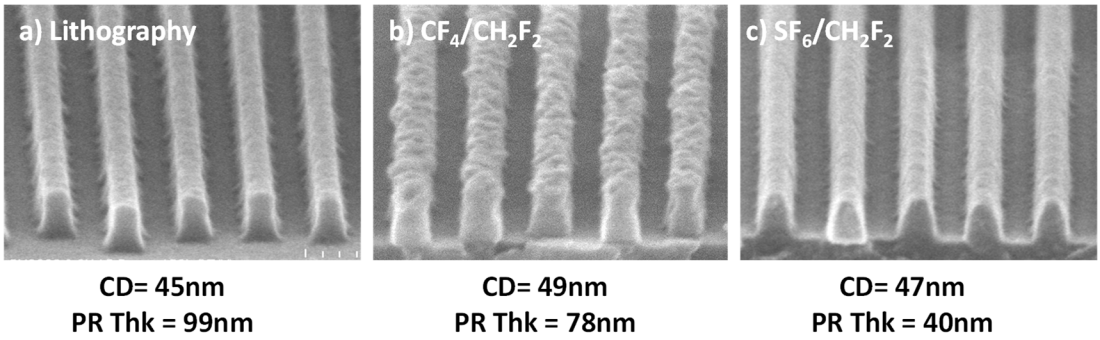

Figure IV-21 SEM Cross section images of Photoresist patterns after a) lithography, b) SiARC open in CF_4/CH_2F_2 (600V, RF<300w, P<10mT) and c) SiARC open in SF_6/CH_2F_2(70V, RF<500ws, P<10mT).

Comparing Figure IV-21(b&c), more tapered photoresist profiles are observed in SF_6/CH_2F_2 conditions than in CF_4/CH_2F_2 conditions. However, the photoresist surface degradation seems to be less important. Similarly, the SiARC profile obtained in SF_6/CH_2F_2 plasma are slightly tapered compared to those obtained in CF_4/CH_2F_2. After full SiARC etching, only 40nm photoresist remain in SF_6/CH_2F_2 conditions compared to the 78nm photoresist left in CF_4/CH_2F_2 conditions, which suggests that the PR/SiARC etch selectivity is lower in SF_6 based plasmas.

b) Roughness transfer in SF_6/CH_2F_2 plasma condition

To measure the LWR and LER evolution during the SiARC etching processes using either CF_4/CH_2F_2 (at 600V) or SF_6/CH_2F_2 (at 70V) plasma chemistries, the CD-SEM and tilted AFM techniques were used. Figure IV-22 shows the LWR and LER evolution measured by CD-SEM.

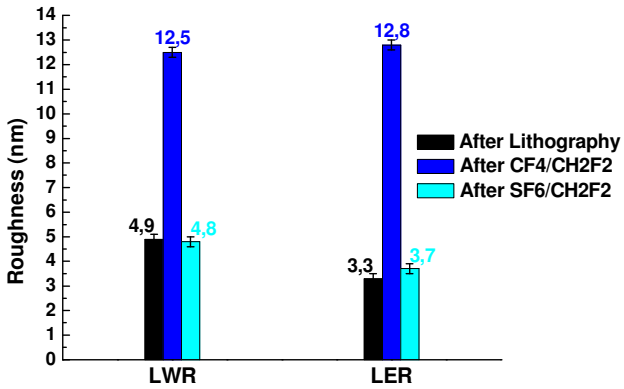

Figure IV-22 Comparison of the SEM roughness values LWR and LER for both SiARC etch conditions, CF_4/CH_2F_2 at 600Vand SF_6/CH_2F_2at 70V.

A strong improvement of the LER and LWR can be observed when the SiARC etch chemistries are changed from CF_4/CH_2F_2 to SF_6/CH_2F_2. The photoresist patterns exposed to SF_6 based plasmas present similar LWR and LER as the reference photoresists.

The AFM measurements of Figure IV-23 confirm the results obtained by CD-SEM analyses and clearly show that in the case of SF_6/CH_2F_2 plasma, the resist LER is not degraded but is even smoothed compared to the initial PR LER, contrary to the case of the CF_4/CH_2F_2 plasma. This resist smoothening

cannot be observed in CD-SEM because the reference PR roughness is underestimated due to the impact of the electron irradiation [1].

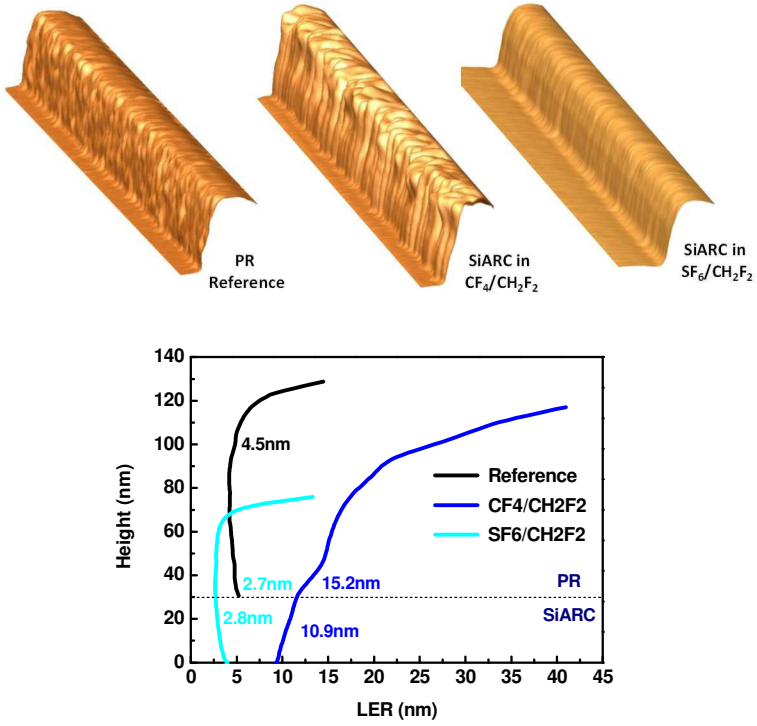

Figure IV-23 a) Tilted AFM images and b) LER profile representations of Photoresist and SiARC patterns after exposure to CF_4/CH_2F_2 (600V)and SF_6/CH_2F_2 (70V)plasma conditions

The averaged LER values were measured for each material, photoresist and SiARC, following the method described in Chapter II. **After exposure to SF_6/CH_2F_2 SiARC etch conditions, the PR LER is decreased from 4.5nm to 2.7nm. The resist smoothing is then transferred into the SiARC layer, resulting in a SiARC LER of 2.8nm, lower than the initial PR LER of 4.5nm.**

These results suggest that the SF_6/CH_2F_2 plasma chemistry is promising candidate for SiARC layer etching without degrading the PR roughness. In the next section, we propose to explain the different mechanisms involved in the etching process of PR films in CF_4/CH_2F_2 and SF_6/CH_2F_2 conditions.

IV.1.2.2 Etch mechanisms of PR and SiARC in SF_6/CH_2F_2 chemistries

a) Photoresist and SiARC etch rates

To compare the SiARC and PR etch mechanisms in CF_4/CH_2F_2 and SF_6/CH_2F_2 based plasmas, both material ER was measured as a function of the applied voltage over full-sheet wafers. The etch rate measurements are plotted as a function of the ion energy square root using Equations 1 described in section IV.1.1.2 [6]:

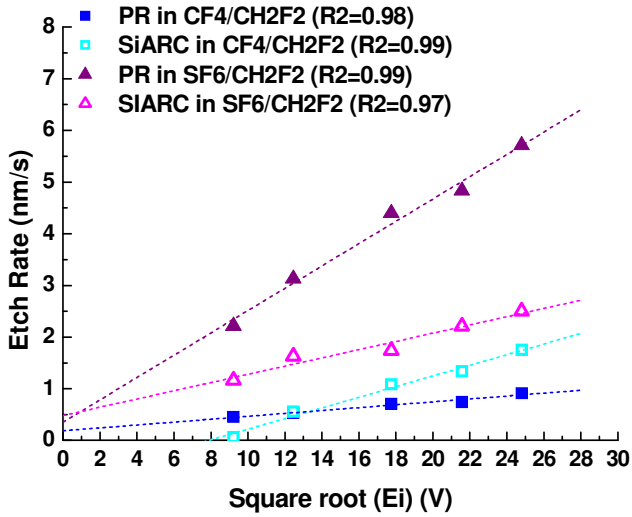

Figure IV-24 PR and SiARC etch rates in CF_4/CH_2F_2 and SF_6/CH_2F_2 plasma as a function of the square root of incident ion energy. The dashed lines represent the linear fit of the obtained data.

In SF_6/CH_2F_2 the PR etch rate is linearly dependent on the ion energy but does not present any energy threshold for the etching to proceed. This suggests that SF_6/CH_2F_2 conditions lead to very reactive plasmas where there is enough fluorine available for PR etching and that the etching is then enhanced by the ion bombardment. On the contrary, in CF_4 plasma, it was found that the PR etch rate was limited by availability of reactive species (i.e. Fluorine) and that the ion bombardment little enhances the PR etch rates.

Concerning the SiARC, the etch rates in SF_6 are higher than in CF_4 but it seems to be less dependent on the ion energy (weaker slope). In fact, for SiARC etching in SF_6/CH_2F_2 plasmas, no energy threshold is observed, which suggests that the plasma is reactive enough to proceed to the material etching without any ion bombardment assistance.

Consequently, the PR/SiARC etch selectivity can be improved in the CF_4/CH_2F_2 plasma by increasing the ion energy, while in SF_6/CH_2F_2 the etch selectivity remains poor for any ion energy.

b) Surface analysis of the PR and SiARC modifications

To confirm the assumptions done concerning the etch mechanism of SiARC and PR in SF_6/CH_2F_2 at 70V compared to the original chemistry in CF_4/CH_2F_2 at 600V, angle resolved XPS (AR-XPS) analysis was carried out following the same experimental protocol proposed in section VI.1.1.3.

- **SiARC surface modifications**

AR-XPS analyses are performed on SiARC surfaces before and after exposure to SF_6/CH_2F_2 and CF_4/CH_2F_2 plasmas for 10s. Figure IV-25 shows XPS spectra of the SiARC extreme surface composition (θ = 76°) before and after plasma exposure. Binding energies of the relevant peaks and the corresponding chemical quantifications are also listed in Table IV-5 and Table IV-6. After SF_6/CH_2F_2 plasma, the C1s, O1s Si2p peak deconvolutions are similar to what has already been described for CF_4/CH_2F_2 in section IV.1.1.2. It should be mentioned that N1s contributions are also present but represent less than 3% of the total quantification and therefore are not considered in our analysis.

Tableau IV-5 Binding energy (eV) and Atomic contribution (%) of the main elements composing the extreme surface reactive layer (θ = 76) of a SiARC sample exposed to $CF_4/CH_2F_2$and SF_6/CH_2F_2 plasmas.

	C1*s*							O1*s*			Si2p			F1s	
Bonding	C-C. C-H	C-CF	C-O-C	C-F	C=O	C-F2	CF3	SiO-C	O-Si	SiO-F	Si-OC	Si-O	Si-OF	F-Si	F-C
Binding Energy (eV)	285.0	286.3	287.0	288.2	289.0	290.4	292.9	532.2	533.2	533.7	102	103.4	104	687.7	688.8
Reference (At%)	26.2	-	1.4	-	-	-	-	6.9	41	-	2.7	21.7	-	-	-
After $CF_4/CH_2F_2$600V (At%)	7.8	10.1	-	6.3	-	2.9	0.4	3.1	16.0	8.8	2.2	10.3	4.1	11.8	16.1
After $SF_6/CH_2F_2$70V(At%)	3.9	3.3	-	3.3	-	3.1	1.1	3.7	25.2	4.6	1.2	10.9	6.5	7.2	23.8

Tableau IV-6 Summary of each element's total atomic contribution at (θ = 76)

Element	C1s	O1s	Si2p	F1s
SiARC Reference (At%)	27,6	47,9	24,4	0
After CF_4/CH_2F_2 600V(At%)	27,5	27,9	16,6	27,9
After SF_6/CH_2F_2 70V(At%)	14,7	33,5	18,6	31

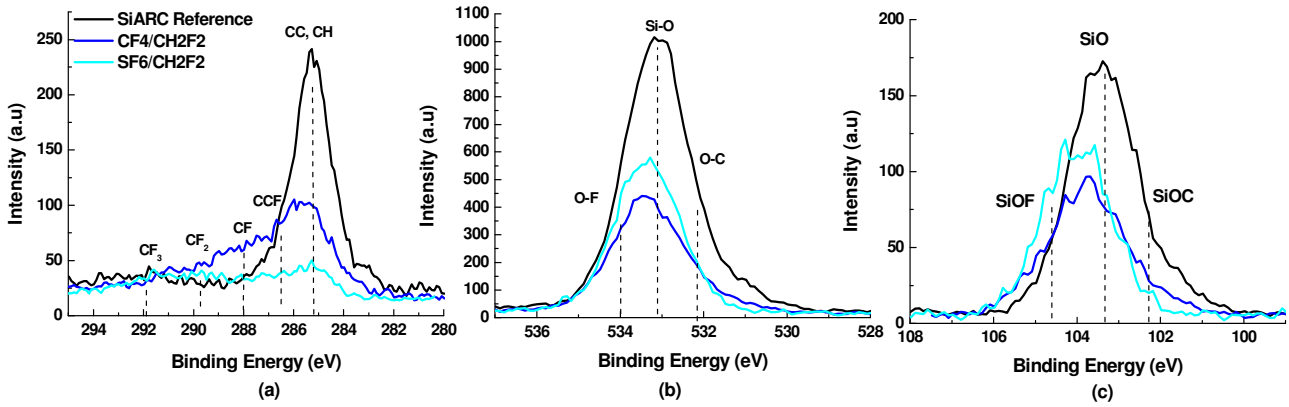

Figure IV-25 (a) C1s (b) O1s and (c) Si2p spectra of a SiARC sample before and after exposure to $CF_4/CH_2F_2$and SF_6/CH_2F_2 plasma conditions. Spectra were taken with an AR-XPS at θ=76° to analyze the contribution of the surface reactive layer. Peaks were shifted according to the C-C or C-H peak at 285eV.

Considering the peaks shown in Figure IV-25 and the chemical quantification of the SiARC extreme surface, we can assume that the main differences between the SiARC surfaces exposed to CF_4/CH_2F_2 and SF_6/CH_2F_2 are a lower carbon concentration (mainly of CC, CCF and CF contributions) and a more important Si, O and F contributions for SiARC surfaces exposed to SF_6/CH_2F_2 plasma conditions.

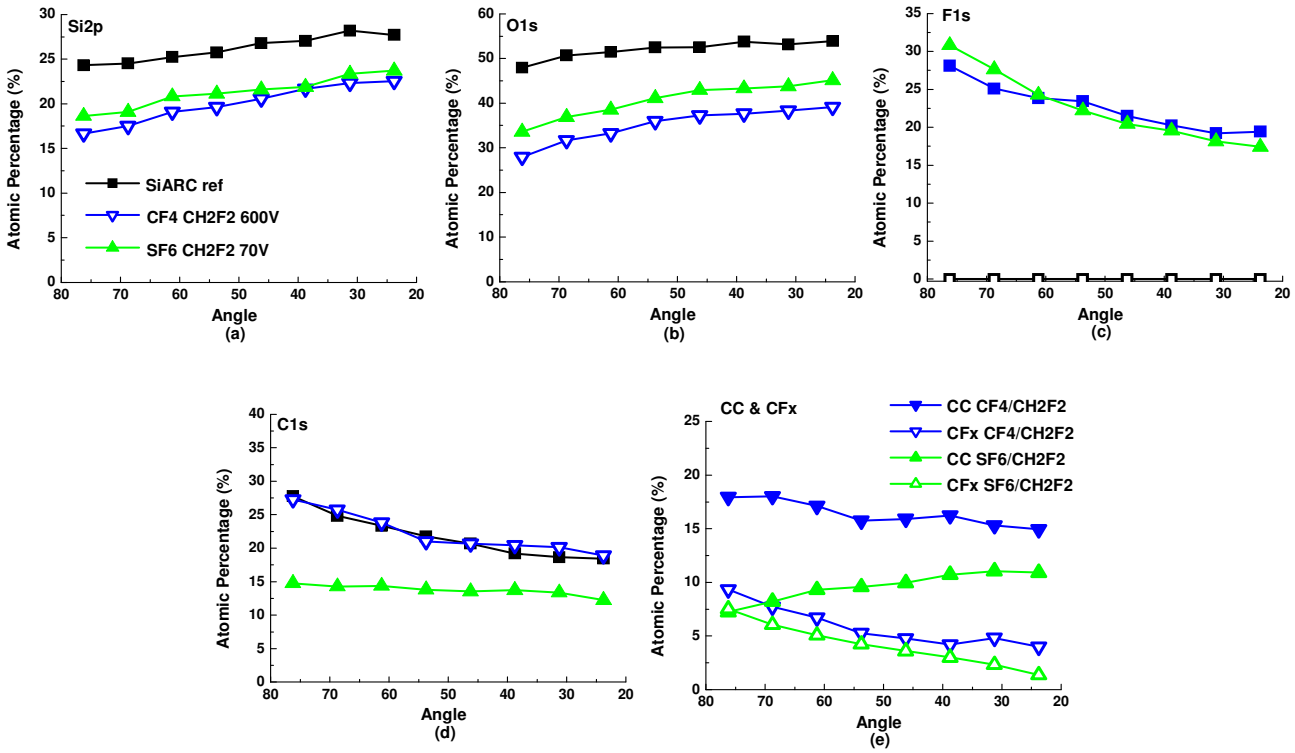

Figure IV-26 Evolution of the SiARC elemental composition as a function of the analyzed angle for SiARC samples before and after exposure to CF_4/CH_2F_2 and SF_6/CH_2F_2 plasmas (a) Si2p; (b) O1s; (c) F1s, (d) C1s and (e) CC and CFx contributions. The C-C and C-CFx contributions have been gathered under the label "C-C", while CF CF_2 and CF_3 contributions are represented by the label CFx.

Figure IV-26 shows the evolution of the SiARC atomic composition as a function angle of analyze for samples exposed to both plasma conditions.

Concerning the Silicon, Oxygen and Fluorine contributions, the evolution of the chemical composition with depth is quite similar for both SiARC plasma chemistries. In both cases, the SiARC surface is depleted in silicon and oxygen which are replaced by fluorine, especially at the extreme surface. The fluorine and silicon concentrations are almost the same for both samples though the oxygen depletion is more important in CF_4/CH_2F_2.

Concerning the carbon, the total carbon concentration decreases from surface to bulk in the case of CF_4/CH_2F_2. This decrease is seen for both CC and CF_x species. For SF_6/CH_2F_2 plasma, the total carbon concentration remains almost constant with depth but the distribution of the carbon species evolves differently: the CF_x concentration decreases with depth in favor of the CC contributions.

To better account of the etch mechanisms of SiARC layers in both plasma chemistries, the Si/C and Si/O and F/C ratios are calculated following the method described in section VI.1.1.3 and plotted as a function of the angle of analyze (Figure IV.27). The Si/C and F/C ratios plotted in figure IV 27 (a & c), are calculated using Equations 3 and 4 as described in Section IV.1.1.2. The SiARC samples are analyzed before and after exposure to plasma conditions.

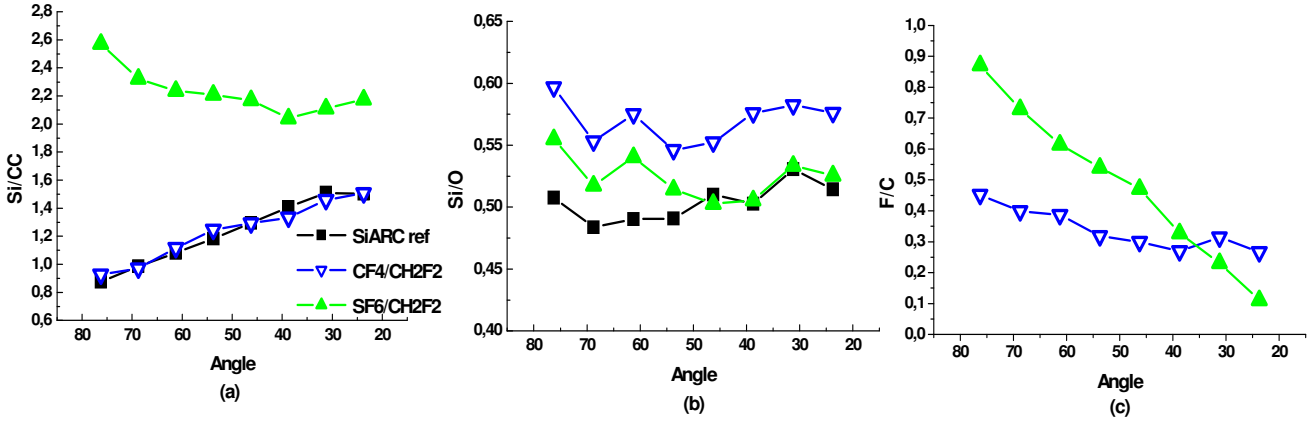

Figure IV-27 (a) Si/CC (measured with equation 3), (b) Si/O and (c) F/C ratios (equation 4)of SiARC samples after exposure to CF_4/CH_2F_2 plasma (at 600V) and SF_6/CH_2F_2 plasma (at 70V)conditions during 10s.

As already observed in Section IV.1.1.2, after CF_4/CH_2F_2 plasma at 600V, the Si/O, Si/C and F/C ratios illustrate a quite homogeneous SiARC reactive layer depleted in oxygen and rich in F with some CF_x incorporated. In this conditions, the strong ion bombardment, contributes to the fluorine depletion and the mixing of the reactive layer.

In the case of SF_6/CH_2F_2 plasma at 70V, the Si/O ratio decreases with the analyzed depth and below a certain angle ($\theta = 50°$) the Si/O ratio becomes similar to that of a reference material. This suggests that the oxygen depletion only occurs at the extreme surface, and is less important than in CF_4/CH_2F_2 plasma. Moreover, the Si/C ratio is much more important after SF_6/CH_2F_2 exposure suggesting a strong SiARC carbon depletion with this process conditions. The F/C ratio is clearly higher than that of CF_4/CH_2F_2 and evolves within the scanned thickness which illustrates a strongly fluorinated SiARC surface. This explains why the etch rates are higher in SF_6/CH_2F_2 than in CF_4/CH_2F_2 at a given ion energy, since enough fluorine is provided by the SF_6 plasma. According to Table 5, in SF_6/CH_2F_2 plasmas the fluorine is preferentially linked to carbon forming F-C bonds while in CF_4/CH_2F_2 it is mixed within the reactive layer and linked to both Silicon and Carbon. This result may explain the increased Si/C and F/C ratios in SF_6/CH_2F_2 plasmas (cf. Figure IV-27).

We can conclude that in CF_4 plasma the SiARC etching proceeds through the presence of a CF_x species that assist the Si-O breaking and lead to oxygen removal (certainly through CO species formation). This helps the formation of Si-F bonds that would subsequently lead to volatile SiF_4 products.

In SF_6/CH_2F_2 plasma, the fluorine mainly reacts with the carbon present in the SiARC layer to form CF_x (x= 1, 2, 3) species and leading to Carbon depletion of the SiARC layer. The breakage of the Si-O bonds and subsequent SiARC Oxygen depletion mainly occurs at the extreme surface certainly because the ion penetration depth is lower at 70V (~1nm) as compared to 600V (~4nm) [19]. In this plasma, the surface is richer in fluorine than for CF_4/CH_2F_2 condition but most of the fluorine is bonded to carbon and few to silicon. In this conditions, the etch rates are limited by the insufficient ion energy for ion mixing. This is consistent with the lower ER obtained with SF_6/CH_2F_2 at 70V compared to those in CF_4/CH_2F_2 at 600V.

- **Photoresist surface modifications**

A detailed analysis of the photoresist extreme surface composition (θ = 76º) is described in Fig. IV.28 and Table 7 and 8.

Samples are fitted considering the peak shift at 285eV attributed to the C-C or C-H contribution of the bulk photoresist. The remaining peaks between 286-293eV are attributed to different fluorocarbon species as described previously for the SiARC samples. However, in the SF_6/CH_2F_2 plasma condition the presence of nitrogen (N_2) and sulfur (S) contribute to the formation of CN and CS species that may deposit over photoresist and SiARC. In the literature, the CN and CS species are referred to appear at 286eV [20] together with the CCF species. Due to this contribution, the remaining fluorocarbon peaks are slightly shifted (~0.6-1eV) towards higher energy values. All species binding energies for each plasma condition are summarized in Table 7. The XPS peaks are fitted following the same procedure as described in section VI.1.1.2.

Tableau IV-7 Binding energies and atomic percentages for each atomic element of a Photoresist exposed to CF_4/CH_2F_2 and SF_6/CH_2F_2 plasma conditions*

	C1s							O1s			F1s			N1s	
Bonding	C-C, C-H	C-CF, C-S & C-N	C-O-C	C-F	C=O	C-F2	CF3	O=C	O-C	O-F	F-C (Poor)	F-C	F-C (rich)	NC	NF
Binding Energy (eV)	285.0	286.2	287.0	288.2	289.0	290.3	294	532.2	533	533.8	687	688	688.7	-	-
PR reference (At%)	44.3	-	10.6	-	12.2	-	-	13.3	10.7	-	-	7.6	-	-	-
CF_4/CH_2F_2 600V (At%)	27.5	16.2	-	12.4	-	7.5	2.1	-	2.5	2.4	24.5	4.9	-	-	-
Binding Energy (eV)	285.0	286.8	-	289.2	-	291.3	293.4	-	533	534.5	-	688.3	689.3	400	401.8
SF_6/CH_2F_2 70V (At%)	10.8	9.8	-	11.2	-	10.0	3.5	-	1.5	1.4	-	27.6	16.7	1.4	4.3

*Note that for all PR samples, 0.5-2% of Sulfur is observed (S2p) which will not be considered in this analysis

Tableau IV-8 Summary of each element's total atomic concentration at (θ = 76)

Element	C1s	O1s	F1s	N1s
PR reference (At%)	67,1	24	7,6	1,3
CF_4/CH_2F_2 600V (At%)	65,7	4,9	29,4	0
SF_6/CH_2F_2 70V (At%)	45,3	2,9	44,3	5,7

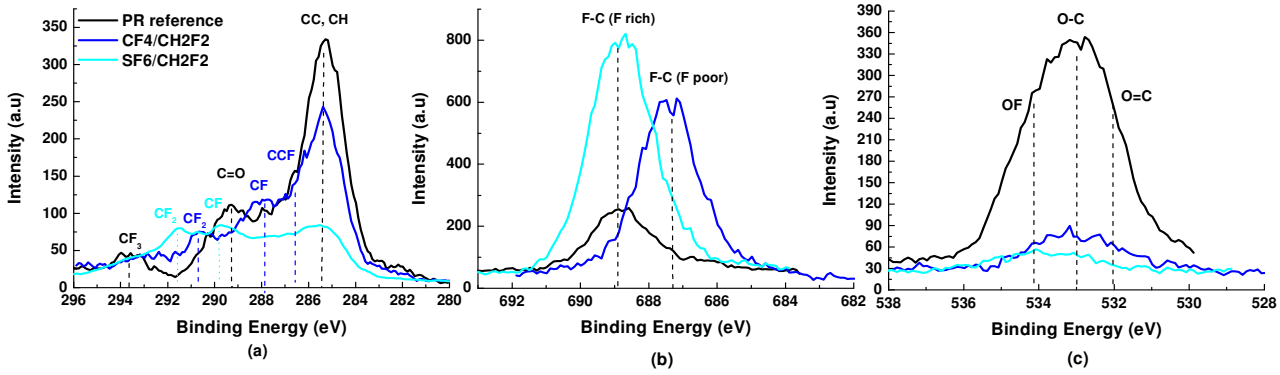

Figure IV-28 AR-XPS (a) C1s, (b) F1s and (c) O1s spectra of a photoresist before and after exposure to CF_4/CH_2F_2(600V) and SF_6/CH_2F_2(70V) plasmas for 10s. Spectra are taken from the extreme surface (θ = 76º)

After both plasma conditions, a photoresist carbon and oxygen depletion is observed. In the case of SF_6/CH_2F_2 exposed samples, a stronger fluorine content is observed which contributes to the enhanced PR carbon and oxygen depletion.

The photoresist composition evolution with depth is also shown in Figure IV-29.

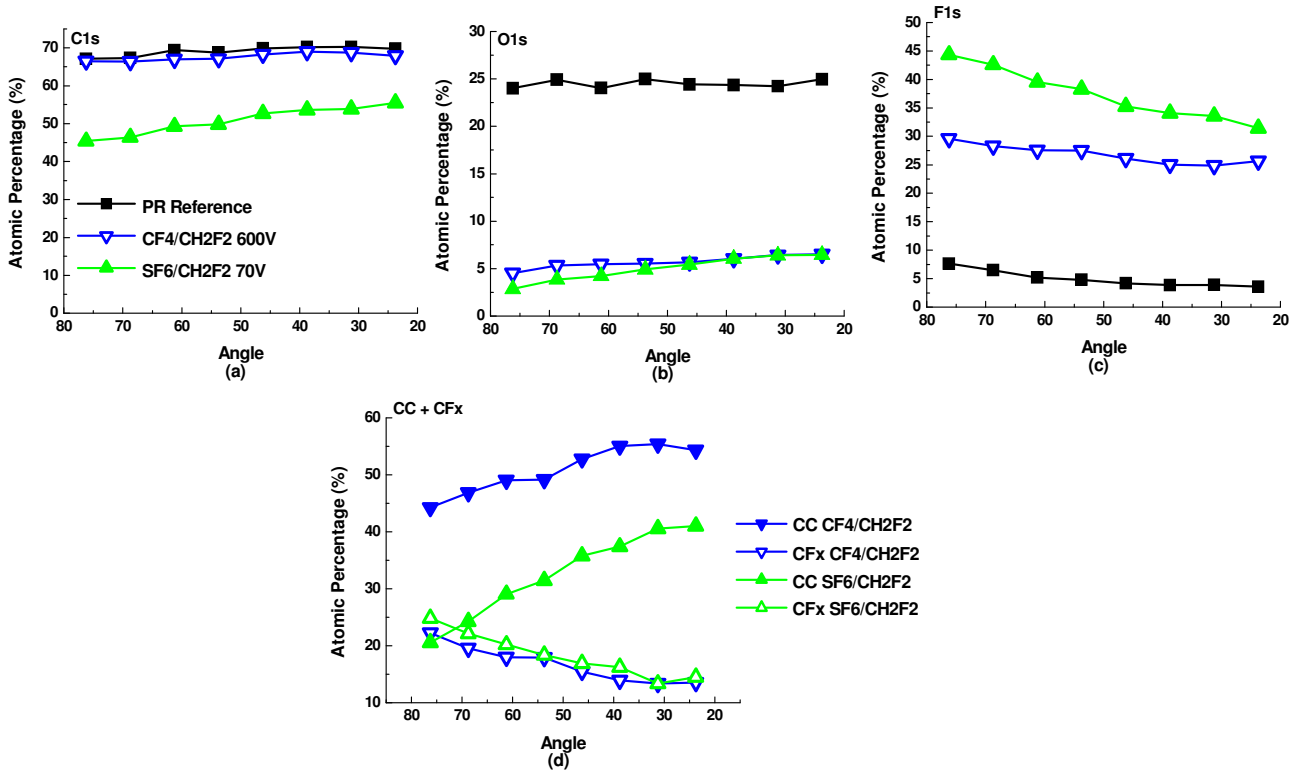

Figure IV-29 Evolution of the Photoresist elemental compositions as a function of the analyzed angle for PR samples exposed to (a) CF_4/CH_2F_2 plasma (at 600V) and (b) SF_6/CH_2F_2 plasma (at 70V).

In CF_4/CH_2F_2, the probed surface is almost homogeneous, with almost constant O, F and C concentration all over the probed depth. A more detailed analysis of the carbon concentration shows a more important CF_x at the extreme surface in detriment of CC contributions.

In SF_6/CH_2F_2, the evolution with depth is more significant. Though the CF_x contribution is almost the same for both chemistries, in SF_6/CH_2F_2 the extreme surface is clearly richer in fluorine and further depleted in carbon and oxygen. The fact that in SF_6/CH_2F_2 we obtain a less homogeneous PR surface with a lower modified depth certainly corresponds to the lower ion penetration depth in SF_6/CH_2F_2 at 70V than in CF_4/CH_2F_2 at 600V.

Figure IV-30 illustrates the evolution of the F/C ratio with depth for a photoresist after exposure to both SiARC etch chemistries.

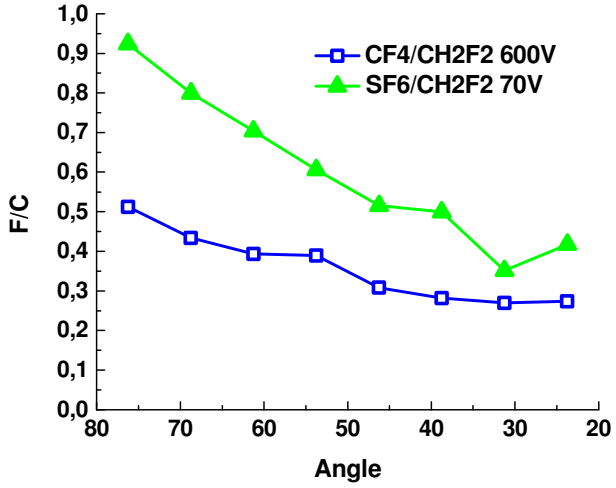

Figure IV-30 F/C ratio as a function of the scanning angle for photoresist samples exposed to SF_6/CH_2F_2 at 70V and CF_4/CH_2F_2 at 600V plasma processes. The ratio is calculated using Equation 4.

While for CF_4/CH_2F_2, the F/C ratio remains uniform over the whole scanned thickness and represents a C-rich FC reactive layer, a significant gradient is observed in the F/C ratio measured over the photoresist exposed to SF_6/CH_2F_2 plasma conditions. This suggests the formation of F-rich reactive layers which are particularly rich in fluorine at the extreme surface. Therefore, in SF_6/CH_2F_2, the etch rates are not limited by the amount of available reactive species as it could be the case in CF_4/CH_2F_2. The CF_x species in SF_6/CH_2F_2 are most likely formed due to the fluorination of the PR (i.e. H abstraction and C-F bonds formation followed by CF_4 etch byproducts) and result in fluorine rich photoresist surfaces. In revenge, in the case of CF_4/CH_2F_2, the CF_x species come from ion implantation and ion mixing, which results in a PR surface that remains rich in carbon.

These XPS analyses reveal that state-of-art- CF_4 based plasma chemistries modify photoresist surface to form a carbon rich CF_x like surface reactive layer (Fig IV-28a). In revenge, angle resolved XPS results show a fluorine-rich photoresist surface in SF_6-type plasmas.

c) Conclusion on the etch mechanisms for both SiARC etch chemistries

Concerning the SiARC etch mechanism, the SiARC etch rate is limited by the amount of carbon and fluorine available for oxygen and silicon depletion and the applied ion energy for Si-O bond breaking. In the case of CF_4/CH_2F_2 conditions at 600V, the SiARC follows an ion enhanced chemical etch mechanism promoted by the implantation and mixing of CF_x (x= 1,2,3) ions. In SF_6/CH_2F_2 based plasmas, the polymerization is reduced, and the SiARC is mainly etched due to fluorine diffusion that enhances carbon removal.

Concerning the photoresist, the resist degradation is due to the contribution of a fluorocarbon deposition and energetic ion sputtering. In CF_4/CH_2F_2 conditions, no good compromise was found where suitable SiARC etch rates are obtained keeping satisfying PR patterns. In SF_6/CH_2F_2 very chemical process conditions are obtained with an excess of fluorine that covers the PR surface. This excess in fluorine prevents from FC deposition and contributes to the chemical etching of Photoresist asperities (such as in trim process, cf. chapter III-section III.3.3.2), resulting in an overall reduced sidewall roughness (Fig IV-23). Another hypothesis for the PR sidewall roughness reduction may be the erosion

of the PR asperities due to reactive sputtering [21] or ion reflection [7]. *Guo et al* proposed a PR smoothening mechanism based on 3D Monte Carlo simulations of the PR profile evolution as a function of the ion bombardment incidence angle **[21].** In their study, they consider that the PR sputtering yield is angle dependent and presents a maximum sputtering yield at 65°. When the PR is exposed to an ion bombardment at the peak etching yield angle for sputtering (~65° in their conditions) the asperities on the PR sidewalls are washed away, resulting in smoother resist sidewalls. Considering the tapered PR profiles obtained in SF_6/CH_2F_2 conditions (Fig. IV-21), this hypothesis could also be considered as a smoothening mechanism in SF_6/CH_2F_2 plasmas. In CF_4, the patterns remain square and are not preferentially sputtered at 65° (certainly because the hard rich in carbon layer formed at the top pattern does not follow the same sputtering behavior with ion incidence), explaining certainly why the smoothening induced by ion sputtering is not observed in this case.

A schematic illustration of the proposed mechanism is shown in Figure IV-31.

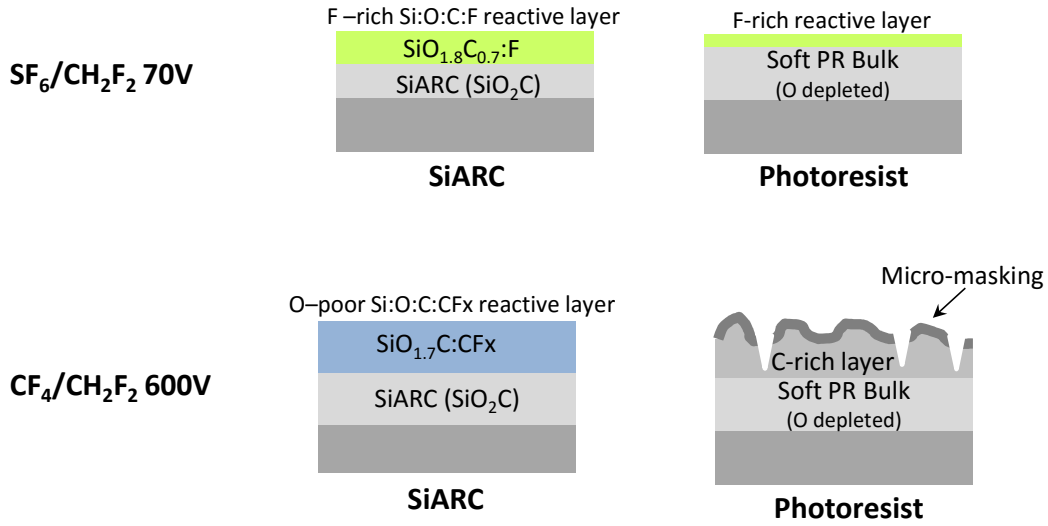

Figure IV-31 Schematic representation of the SiARC and Photoresist etch mechanisms in CF_4/CH_2F_2 and SF_6/CH_2F_2

The SiARC etch process in SF_6/CH_2F_2 seems a good candidate for gate patterning. However, due to the increased PR etch rate in SF_6 based plasmas, the PR budget may become a challenge for the application of these processes in real gate integrations, mostly when long trim or SiARC over-etch steps are required.

The LAM Ex reactor presents another parameter that can contribute to optimize the process, the possibility of working in a Bias Pulsing (BP) mode. Figure IV-32 illustrates PR/SiARC gate patterns exposed to equivalent to SF_6/CH_2F_2 SiARC etch conditions in a continuous wave (CW) and Bias Pulsing (BP) mode. For this test, a final gate CD of 20nm was targeted, and therefore an equivalent trim time of 72s was used for both samples.

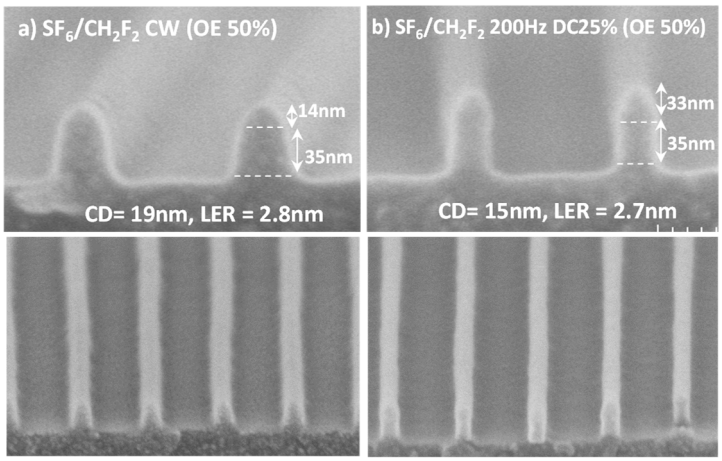

Figure IV-32. SEM Cross-Section images of PR/SiARC stacks exposed to SF_6/CH_2F_2SiARC conditions in a (a) Continuous wave, and (b) Bias pulsing mode.

With bias pulsing, the PR budget is strongly improved while keeping equivalent LER values. With these conditions, well defined SiARC patterns are obtained even for very long trim times. Further details on this study is presented in Annex II.

IV.2 Pattern transfer into gate stack (HM/Silicon/TiN)

As shown in the previous sections, it is important to control gate patterning from the very beginning by controlling the polymer/plasma interactions and optimizing the SiARC etch steps. However, patterning improvements obtained at the tri-layer stack (PR/SiARC/SoC) need to be maintained through the whole gate patterning process. Therefore, the roughness evolution along the whole gate etch process needs to be evaluated.

IV.2.1 Impact of SiARC etch process in the LER transfer for HKMG patterning

The AFM technique is used to study the LER transfer during the gate patterning and to evaluate the impact of the used SiARC etch process on the final gate LER. For this purpose, AFM is carried out on photoresist patterns after lithography, then after the SiARC etch process using either CF_4/CH_2F_2 or SF_6/CH_2F_2, and finally after the whole gate stack process (comprising the SoC/HM/Silicon/TiN etch), as shown in Figure IV-33. It should be reminded that the PR/SOC/SiARC layers are removed after the HM etching step, explaining why the final pattern investigated is composed of only the HM/Polysilicon/TiN stack. Averaged LER values for all the materials involved in the stack (photoresist, SiARC, HM, polysilicon and TiN) are extracted from figure IV-33 (a&b) and reported in figure IV-33c that compares the LER transfer during gate patterning for the two SiARC etch plasma chemistries investigated.

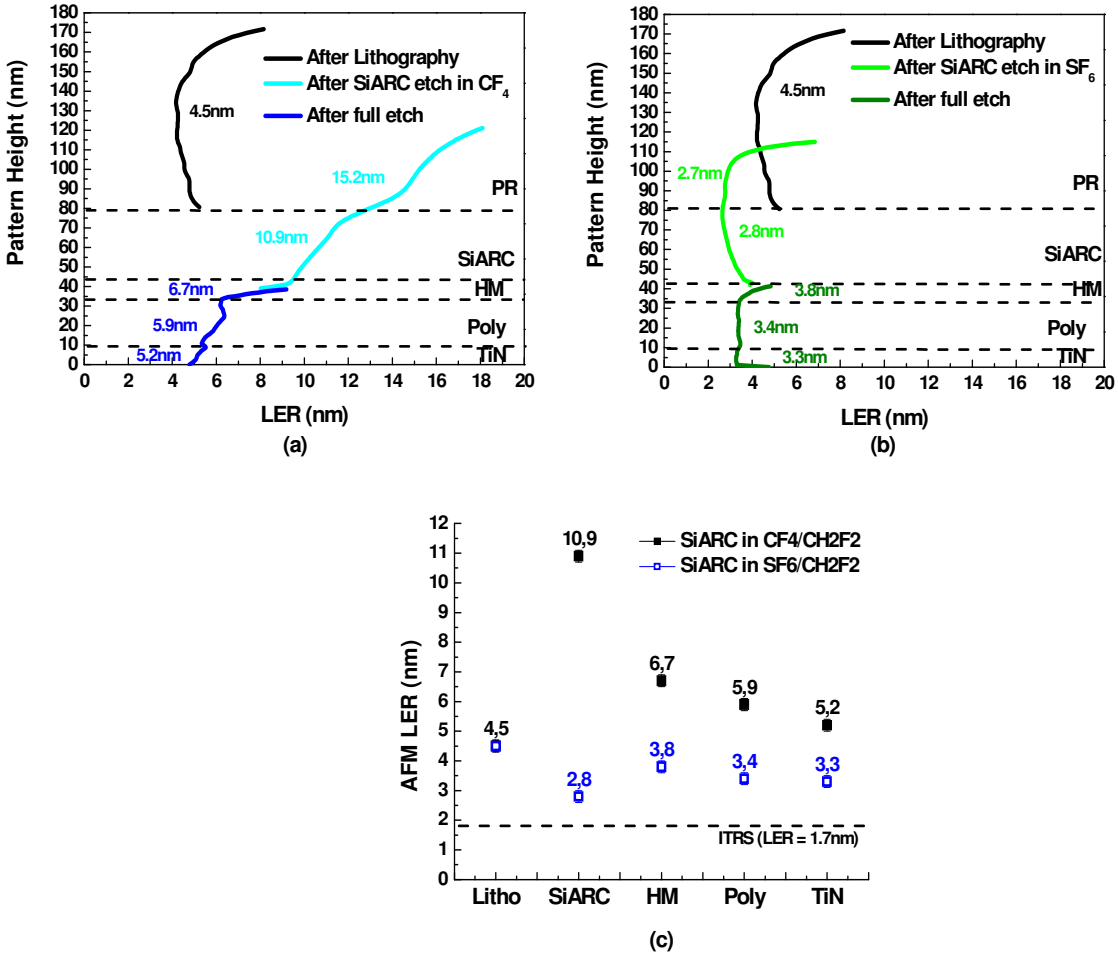

Figure IV-33 Comparison of the LER evolution during gate patterning for the two different gate etch processes: (a) SiARC etch in $CF_4/CH_2F_2$and (b) SiARC etch in SF_6/CH_2F_2. The remaining gate etch process remains the same for both samples. (c) Comparison of LER values obtained in (a) and (b) after each process step is shown.

As shown in Figure IV-33a, if the CF_4/CH_2F_2 plasma chemistry is used for SiARC etching, the SiARC LER value is strongly increased to 10.9nm compared to the initial photoresist LER of 4.5nm (as already explained in previous sections). However, after the whole gate patterning, the LER values of the polysilicon and TiN layers are decreased down to 5.9nm and 5.2 nm respectively. It is also interesting to highlight the fact that after the whole gate patterning, the LER decreases from the top of the pattern to the bottom leading to slightly lower LER value in TiN than in Polysilicon. To better understand this trend, CD-SEM analyses using the PSD fitting method are also carried out on the same patterns. Figure IV-34 shows the PSDs obtained after the lithography, SiARC etching step and finally after silicon etching for both SiARC etch plasma investigated. It should be reminded that the roughness measured after SiARC etching by CD-SEM is overestimated since it takes into account an average roughness along all the pattern sidewalls and it is clearly observed in Figure IV-33a that the LER is not at all constant along the pattern height and that the SiARC LER at the very bottom (9.8nm) is lower than the average LER value given by AFM (10.9nm).

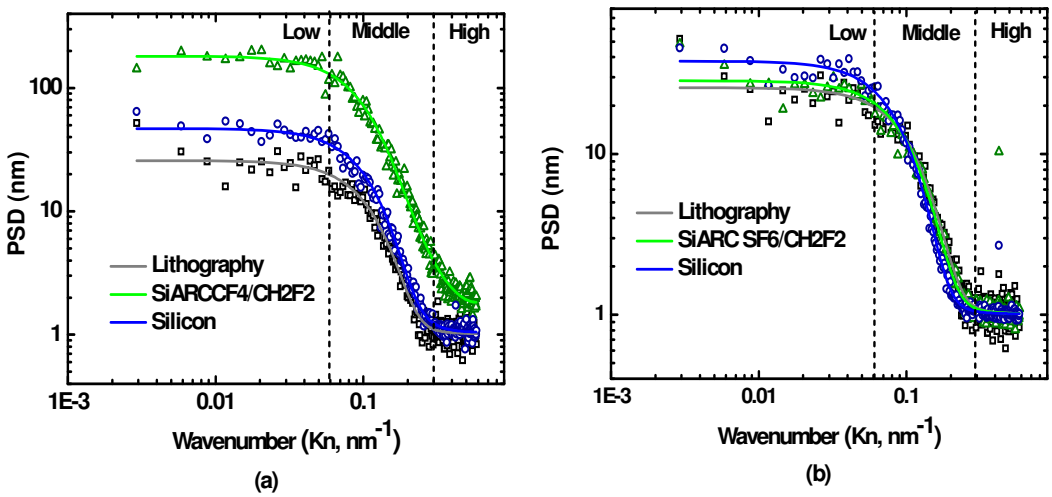

Figure IV-34 Spectral analysis of the roughness evolution during the gate etch process with a SiARC etch chemistry in (a) CF_4/CH_2F_2 and (b) SF_6/CH_2F_2.

The spectral analyses of the roughness after SiARC etch condition in CF_4/CH_2F_2 (Fig IV-34a) show that the SiARC etching introduces roughness on all the frequency range. Then, after gate etch process, the roughness is significantly reduced in all the frequency range but has been increased compared to the roughness of the initial PR pattern, especially in the mid-low frequency region [2]. Other authors have also observed that roughness could be decreased during plasma transfer. They showed that all the roughness frequencies are not equally transferred during plasma etching processes. More particularly, the high frequency roughness components are lost during the pattern transfer steps. The reason for not transferring this high frequency roughness during plasma transfer is not completely clear. It is suggested that the bumps on the sidewalls generating the roughness at small scale are sputtered by the energetic ion arriving at grazing incidence before being transferred.

Optimization of the SiARC etch step from CF_4/CH_2F_2 based plasmas towards less polymerizing and less energetic plasma conditions in SF_6/CH_2F_2 leads to a strong improvement of the LER values in PR and SiARC (Fig IV.33b). However, after the whole gate patterning, the LER values obtained in the HM, Polysilicon and TiN layers are 3.8nm, 3.4nm and 3.3nm respectively, slightly higher than the initial SiARC LER value of 2.8nm. This increased LER is also observed in Figure IV-34b, where after full patterning, the low frequency roughness components have been increased. This increase of the sidewall LER is suspected to occur during the HM opening step in fluorocarbon chemistries and would be then partially transferred into polysilicon and TiN. To support this hypothesis, further studies were carried over gate patterns etched with different HM opening chemistries. The results will be discussed in Section IV.2.3.
Anyway, although the LER is slightly degraded during the polysilicon etch process, the final TiN roughness in the optimized gate etch condition in SF_6/CH_2F_2 remains low (3.3nm) compared to the LER of 5.2nm obtained with the original process.

Other roughness parameters can also be extracted by CD-SEM metrology, such as the correlation factor, that can help us to better characterize the roughness evolution during the gate etch process. The correlation factor tells if the edge fluctuation for each pattern side is independent and varies randomly (i.e. no correlation) or if both edge positions are dependent and vary in a simultaneous manner (i.e. correlated sidewalls) (cf. Chapter I). Figure IV-35 shows SEM cross-section images that illustrate the impact of the correlation factor over Silicon gate patterns.

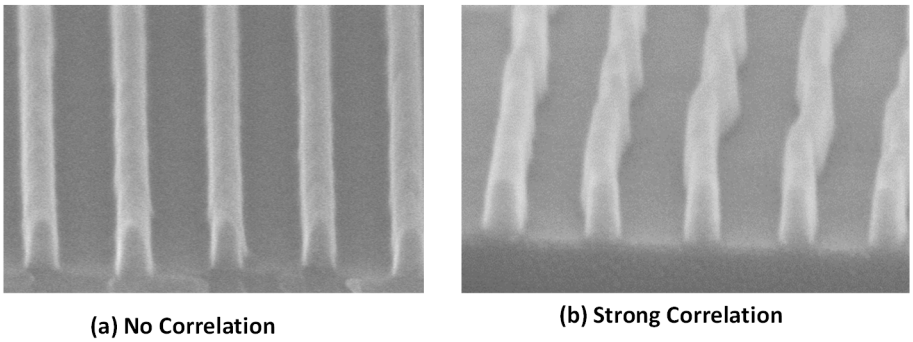

Figure IV-35 SEM Cross-Section images of Silicon gate patterns with (a) No sidewall correlation and (b) Strong sidewall correlation.

Figure IV-36 illustrates the evolution of the correlation factor during the gate etch process. The correlation factor is measured after lithography, after SiARC etching in CF_4/CH_2F_2 and SF_6/CH_2F_2 conditions and after the whole gate patterning, which includes SoC, HM, Silicon and TiN etch steps. The comparison of the correlation factor evolution as a function of the applied SiARC etch chemistry is shown in Figure IV.36.

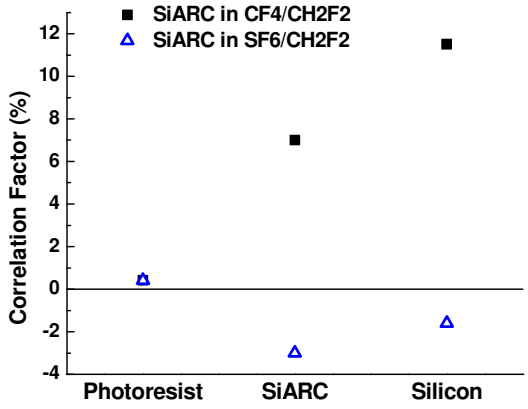

Figure IV-36 Comparison of the correlation factor evolution as a function of the applied SiARC etch chemistry

It should be considered that no roughness information of SiARC and Silicon can be obtained by CD-SEM. Therefore, after SiARC etching, the correlation factor is not measured directly over SiARC but over remaining PR layers. The same occurs after full etch process, where the correlation factor is measured over remaining SiO_2 hard-mask instead of silicon. However, it can be observed that an evolution in the correlation factor occurs within the PR/SiARC stack during the SiARC etch steps in CF_4/CH_2F_2 that is transferred and incremented during the gate stack etching process. Such evolution is not observed after SiARC etching in SF_6/CH_2F_2 conditions, where the correlation values even become negative after SiARC opening or full etch. The measure of negative correlation values after SiARC etching in SF_6/CH_2F_2 is not very clear. Negative correlation values could be attributed to sidewall roughnesses that are "anti-correlated" to each other (see Chapter I). However, a 0-2% variation in the correlation factor is not enough to assure any process variation, and is more likely due to a metrology incertitude.

According to what it has been reported in the literature, the increase of the correlation factor is attributed to a wave-like mask degradation phenomenon reported as "wiggling" [22] [23].

The first report was provided by *Darnon et al* [22] who studied the deformation of SiOCH patterns etched in fluorocarbon based plasmas using a TiN hard mask. It was proved that the pattern deformation depends on the compressive stress of the hard mask. The SiOCH cannot assess the

relaxation of the residual stress of the TiN HM due to its poor mechanical stability and therefore the pattern is deformed during the etch process to limit the constraints. *Darnon et al* and *Ducoté et al* [22] [23] proved that the deformation degree depends on the pattern geometry (i.e. aspect ratio) the mechanical properties of SiOCH and TiN HM structure and residual stress.

In our case, the increased correlation factor is already observed over PR/SiARC stacks, which do not include stressed TiN HM layers and do not present strong aspect ratios.
We suspect that the formation of a C-rich CFx layer (graphite-like) at the top of the resist pattern in CF_4/CH_2F_2 conditions stresses the photoresist which relaxes the constraints by wiggling formation during the SiARC etch process. This wiggling certainly explains why the roughness increases significantly in the mid-low frequency range as observed in Figure IV-34. Afterwards, the wiggling effect may be increased during the 135nm SoC layer etching, due to the high aspect ratios obtained and the poor mechanical stability of SoC materials. This phenomenon results in stronger correlation factors measured over HM/Silicon/TiN gate stacks and the presence of mid-low frequency components after gate etching (cf. Figure IV-34). In SF_6/CH_2F_2 SiARC etch conditions, the excess of fluorine and the applied low bias voltages prevents the PR graphitization which may limit the wiggling effect and explain the lower correlation factors measured after SiARC etching.

In conclusion, the modification of the SiARC etch condition from the standard process in CF_4/CH_2F_2 towards a less polymerizing and less energetic SF_6/CH_2F_2 chemistry limits the wiggling phenomena in the PR/SiARC stack and results in lower LER values over the full gate stack.

Changing to SiARC process conditions in SF_6/CH_2F_2 seems necessary for successful gate patterning. However, the LER values obtained with the optimized SiARC process conditions (3.3nm) still do not reach the specifications defined by the ITRS 2012 (Fig IV-33c) [24]. Further process optimization will be required to meet the defined standards.

IV.2.2 Impact of Trim step addition in the LER transfer for HKMG patterning

The SiARC etch process optimization is not enough to ensure good LER values in Polysilicon and TiN. Further smoothening of the PR/SiARC roughness is required to meet the expectations of the semiconductor industry. In Chapter III, we outlined the interest of adding Cl_2/O_2 based trim steps for the improvement of the PR LER. Such steps are already integrated in our standard etch recipes to adjust the PR CD. According to our studies, the PR LER is decreased from 4.5nm to 2.2nm after a trim treatment of 40s. In this section, we evaluate the impact of trim step addition into the final gate LER. Note that, as discussed in Chapter III, trim steps followed by SiARC etch processes in CF_4/CH_2F_2 are detrimental for the PR and SiARC LER (Trimmed resists behave similarly as reference resists upon CF_4/CH_2F_2 SiARC etching process). Therefore, in this section, we will only discuss about trim steps combined with SiARC etch processes in SF_6/CH_2F_2 chemistries.

For this, photoresist patterns were measured by AFM with and without exposure to Cl_2/O_2 trim steps for 40s. Note that, during trim steps, the PR pattern is vertically eroded, which explains the differences in the scanned pattern height for both process conditions (Figure IV-37a&b). Then, both samples were exposed to a SiARC etch step in SF_6/CH_2F_2 process conditions. The SiARC patterns are then transferred into the full gate stack (HM/Silicon/TiN) using the same process conditions for both samples. The LER evolution was measured over photoresist (after lithography, trim and SiARC etching), over SiARC layers (after SiARC etching) and over the full gate stack (HM/Silicon/TiN) after full process (Figure IV-37a&b).

The obtained averaged LER values are extracted from figure IV-37 (a&b) and reported in Figure IV-37c that compares the LER transfer during gate patterning for trimmed and untrimmed photoresists.

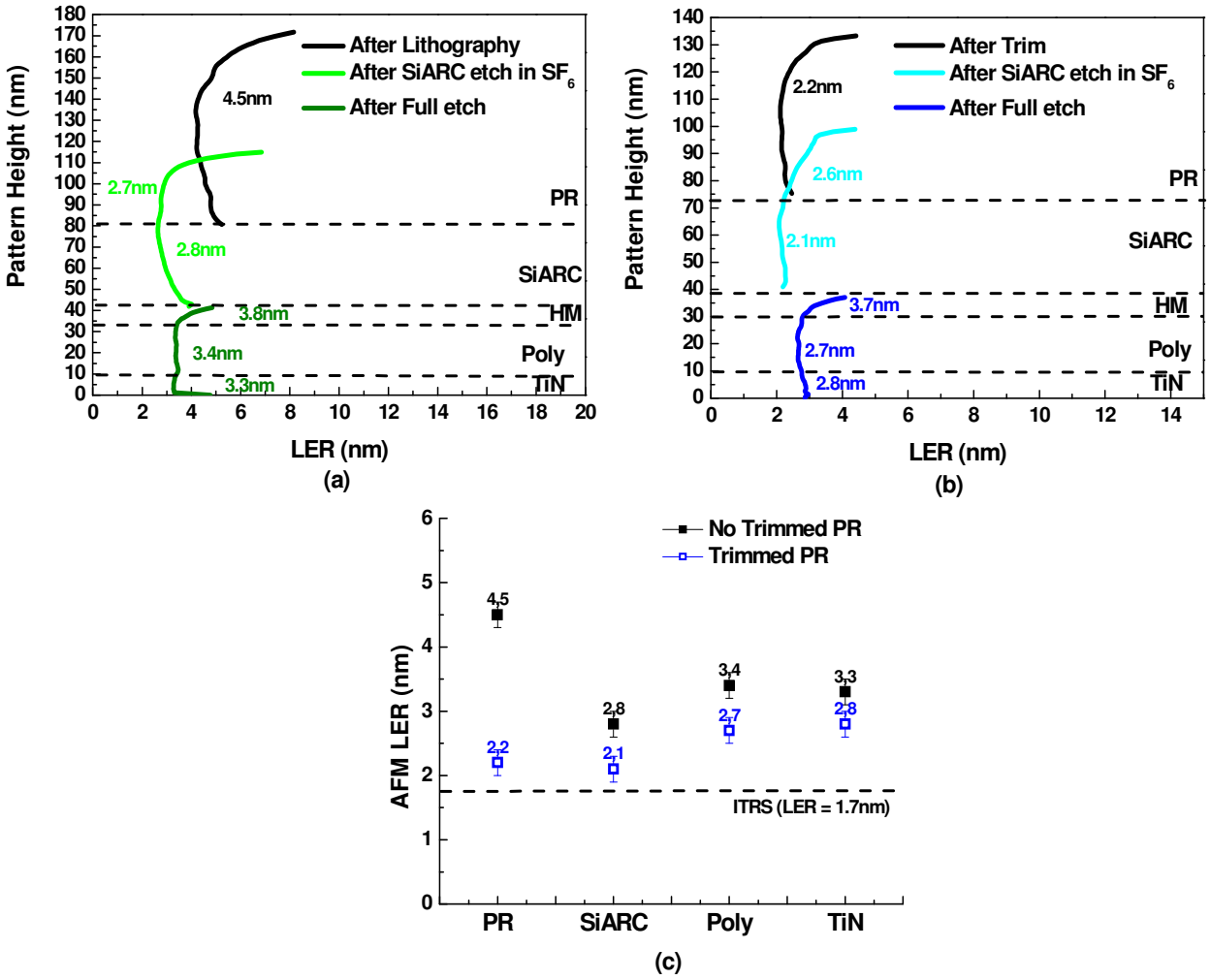

Figure IV-37 Comparison of the LER evolution during gate patterning: (a) samples. (c) Comparison of LER values obtained in (a) and (b) for each material is shown.

As shown in Figure 37a, the reference photoresist presents an LER of 4.5nm which is reduced to 2.8nm during the SiARC etch step in SF_6/CH_2F_2 conditions. As explained in section IV.2.1, a slight increase of the sidewall roughness is observed after full gate etching, which results in LER values of 3.4 and 3.3nm measured over Polysilicon and TiN respectively.
Addition of trim steps, smoothes the photoresist roughness from 4.5nm to 2.2nm, which is then transferred into the SiARC layer without further modifications (Figure IV-37b). However, this smoothed roughness evolves during the gate etch process and slightly higher LER values of 2.7nm and 2.8nm are measured over polysilicon and TiN respectively. Despite of this slight LER increase during the gate patterning, the final gate LER is significantly lower when trim steps are introduced than without any photoresist trim.

Further analysis of the roughness evolution was carried out by CD-SEM. Figure IV-38 shows the evolution of the correlation factor with gate etch process for photoresists with and without exposure to a Cl_2/O_2 trim condition during 40s. In section IV.2.1, we demonstrated that the correlation evolution

was mainly observed over patterns carried out with a SiARC process condition in CF_4/CH_2F_2. Therefore, for further comparison, the photoresist patterns where exposed to SiARC etch processes either in CF_4/CH_2F_2 or in SF_6/CH_2F_2. Finally, the SiARC patterns were fully transferred into the gate stack following the same process conditions for all analyzed samples. The correlation factor was measured after trim, after SiARC etching and after the whole gate patterning with reference and trimmed resist.

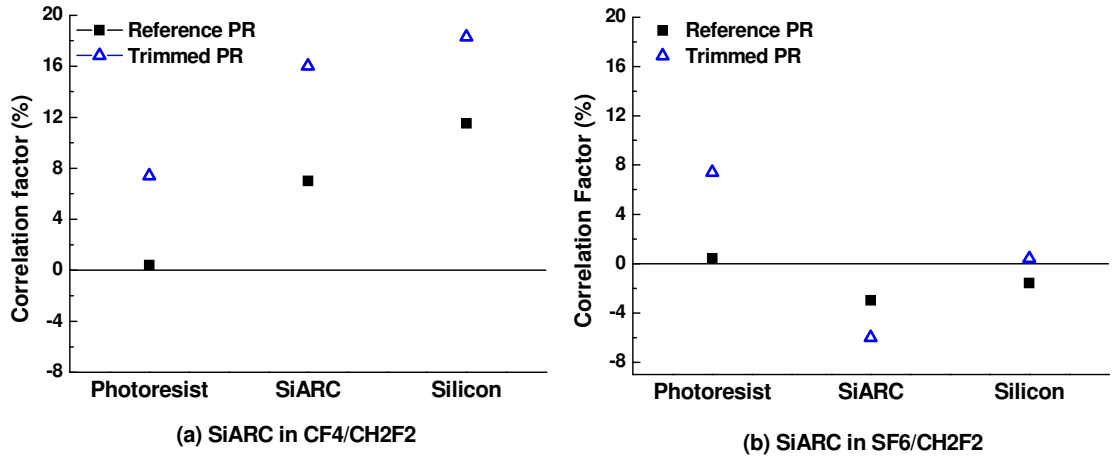

Figure IV-38 Evolution of the correlation factor during gate patterning with or without introduction of Cl_2/O_2 trim condition during 40s for two SiARC etch conditions in (a) CF_4/CH_2F_2 and (b) SF_6/CH_2F_2. For each graph, the correlation factor is measured after lithography (or trim), after SiARC etching and after the whole gate patterning, with or without trim

As shown in Figure IV-38 (a&b), after exposure to Cl_2/O_2 trim steps, photoresist patterns present higher correlation values as compared to reference photoresist. This correlation increase may be attributed to an increase residual stress within the photoresist pattern after exposition to halogen plasmas. The stress generation on PR patterns by exposure to plasma conditions has already been reported in the literature. *Kikutani et al* based on the work done by *Sakai et al* proved that during the SoC etching process in fluorocarbon based plasmas, fluorine diffuses in the SoC pattern and substitutes C-H bonds by C-F bonds [25] [26]Fluorine being a bigger atom than hydrogen, the SoC fluorination leads to an increase of the material volume that induces internal stress and degradation. This mechanism has been reported for a number of organic materials [26] [25] [27]and could be the responsible of the increased pattern deformation (i.e. correlation) after exposure to Cl_2/O_2 plasmas.

This correlation will then evolve differently depending on the SiARC etch step chosen for pattern transfer. If SiARC etch conditions in CF_4/CH_2F_2 are used (Figure IV-38a), a continuous increase of the correlation factor is seen during the gate etch process. As discussed in the previous section, this increase in the correlation values during this step is attributed to a photoresist stress relaxation by pattern deformation, i.e. wiggling. The wiggling effect is known to be amplified with increasing aspect ratios [22]. Thus, it is not surprising that higher correlation values are observed over trimmed samples, where higher pattern aspect ratios are obtained (Figure IV-39).

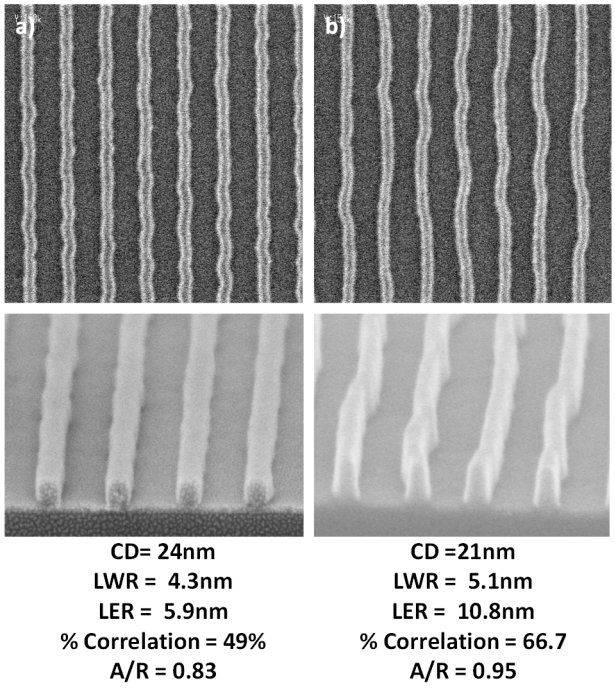

Figure IV-39 Comparison of the Correlation factor and wiggling effect observed over silicon patterns as a function of the gate pattern aspect ratio for two gates etched using the SiARC etch condition in CF_4/CH_2F_2

If the photoresist pattern is transferred into polysilicon using a SiARC etch condition in SF_6/CH_2F_2, relatively low correlation values are observed for either trimmed or reference samples (Figure IV-38b). This suggests that no wiggling deformation occurs during the SiARC etching step (or subsequent SOC etching step) even for samples previously exposed to trim conditions. As already explained, PR exposed to SF_6/CH_2F_2 processes are assumed to be less stressed than those exposed to CF_4/CH_2F_2. Besides, the poor PR/SiARC selectivity in SF_6 based plasmas limits the remaining PR budget which reduces the PR/SiARC pattern aspect ratio. Contribution of both factors prevents gate stack from wiggling even when long trim steps are applied.

As an example, Figure IV-40 shows SEM top view images of gate patterns carried out using both SiARC etch conditions and transferred into Silicon. Trim steps were adjusted to obtain 24nm silicon gate patterns in both cases.

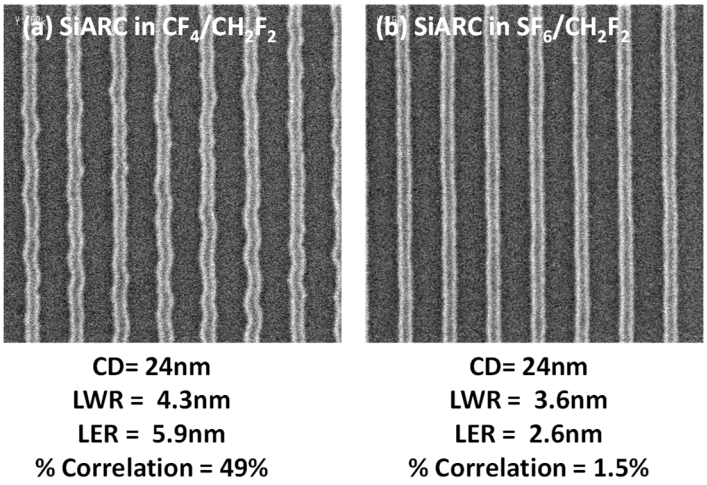

Figure IV-40 SEM top view images of 24nm Silicon gate patterns carried out with SiARC etch chemistries in (a) CF_4/CH_2F_2 and (b) SF_6/CH_2F_2.

Top view SEM images illustrate that for the latest gate integrations, where long trim steps are required to obtain the targeted CDs the standard SiARC etch process in CF_4/CH_2F_2 is not adapted for gate patterning. **Changing the SiARC etch chemistry to SF_6/CH_2F_2 based plasmas, allows correcting the gate's sidewall roughness, which is reduced from 5.9nm to 2.6nm. This improved patterning process also allows carrying out gate patterns with no wiggling effect even when very small pattern dimensions are targeted. This means that the proposed process is also adapted for the patterning of gate features for advanced technological nodes.** Although addition of trim steps and modification of the SiARC etching steps contributes to the photoresist smoothening and improves the gate final roughness, this strategy is not enough to meet the ITRS expectations in terms of LER (LER = 1.7nm). In the previous section, it has been observed that the gate LER increases during the HM/Polysilicon/TiN etch process.

In section IV.2.1 we suggested that the increase of the polysilicon roughness may arise from the HM etch process in fluorocarbon plasmas. In the following section, we will study the impact of the HM etch chemistries on the gate stack LER.

IV.2.3 Impact of HM etch process in the LER transfer for HKMG patterning

IV.2.3.1 Process conditions

In our gate integrations, the polysilicon is patterned using a simple oxide HM that is etched with the same CF_4/CH_2F_2 plasma chemistry used to etch the SiARC layer. However, as described in Chapter I, at ST Microelectronics the 14FDSOI gates are defined using a double hard mask composed of a SiO_2 layer deposed over a Si_3N_4 layer (Fig IV-41). For these integrations, the photoresist patterns need to be efficiently transferred into the oxide HM without impacting the Si_3N_4 under layer. Therefore, HM etch processes that offer a good SiO_2/Si_3N_4 selectivity are required. In our integrations, though this is not necessary, we decided to change the SiO_2 HM etch chemistry towards a more selective one to determine the impact of the HM etch process in the gate LER transfer.

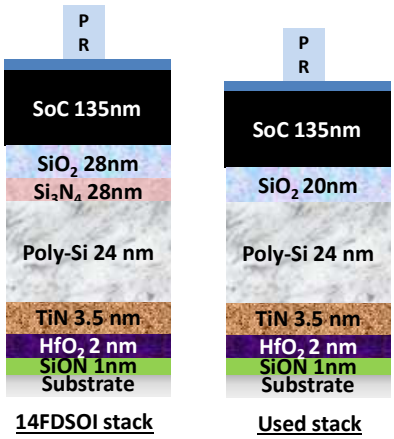

Figure IV-41 Comparison of the 14FDSOI gate integration and our gate integration

In our standard SiO_2 opening process in CF_4/CH_2F_2, the selectivity is very poor as given in Figure IV-42b. A way to increase the etch selectivity of SiO_2 over Si_3N_4 in FC plasma chemistries is to increase the FC polymer formation. As reported by *Rueger et al* and *Standaert et al* [14] [12] the FC film contributes to the SiO_2 oxygen depletion by formation of volatile byproducts such as CO, CO_2 and COF_2 [12]. The same reactions were reported for Si_3N_4 by *Schaepkens et al* who identified nitrogen depletion by formation of volatile compounds such as CNF and FCN [11]. However, the depletion reactions occurring over Si_3N_4 substrates are less efficient than those in SiO_2 [11]and therefore the SiO_2/ Si_3N_4 selectivity can be controlled by promoting plasma polymerizing conditions.

To increase the polymerization in CF_4/CH_2F_2 plasmas, several process modifications can be done, such as, increasing the CH_2F_2 composition in the gas mixture, decreasing the ion sputtering or increasing the working pressure. According to these studies, the CF_4/CH_2F_2 process was modified into an optimized condition at higher working pressures and with lower ion energies. The etch rate and SiO_2/ Si_3N_4 selectivities obtained with this optimized process condition are shown in Figure IV-42 and confirm an improved selectivity with the optimized oxide etch process in CF_4/CH_2F_2.

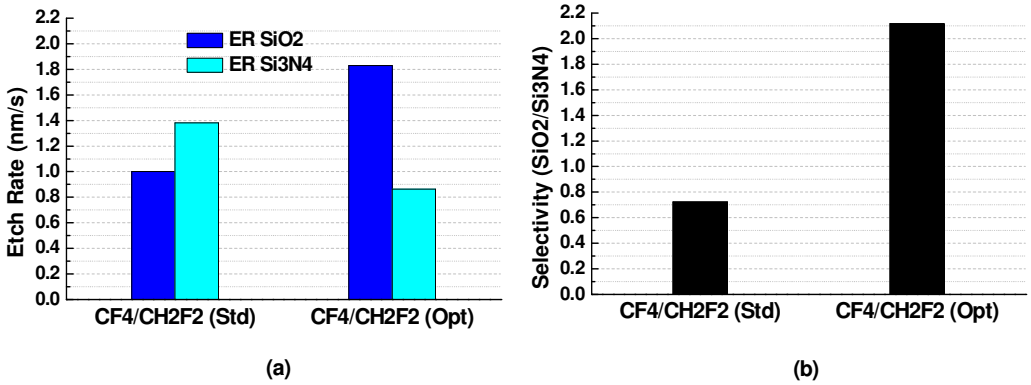

Figure IV-42 SiO_2 and Si_3N_4 hard mask (a) etch rate and (b) selectivity for the standard CF_4/CH_2F_2 process and the optimized process

IV.2.3.2 Roughness improvement with the HM chemistry

To study the impact of the SiO_2 HM process conditions on the final gate LER, the AFM technique is used. Figure IV-43 illustrates the sidewall LER evolution of trimmed photoresist exposed to SiARC etch conditions in SF_6/CH_2F_2 and transferred into silicon with two different SiO_2 hard mask open conditions, the standard process in CF_4/CH_2F_2 and an optimized analog at higher pressures and source powers.

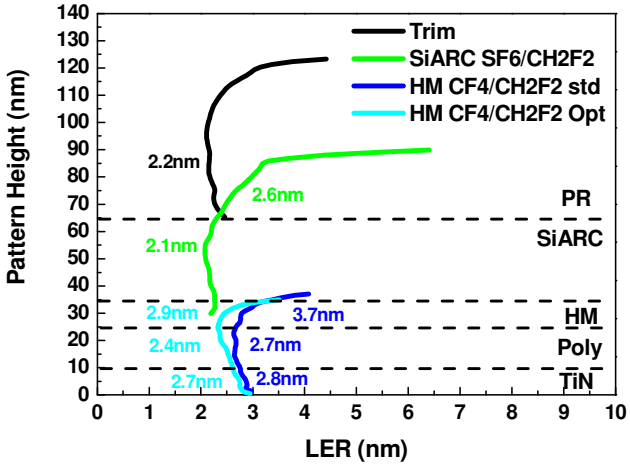

Figure IV43-LER roughness transfer for a gate patterned with a 40s Cl_2/O_2 trim, SiARC open in SF_6/CH_2F_2 and two different CF_4/CH_2F_2 chemistries for SiO_2 hard mask opening

It can be observed that resist trimming lead to smooth photoresist patterns with an LER of 2.2nm which is directly transferred into SiARC resulting in LER values of 2.1nm (as already observed). In the standard process, the roughness is strongly degraded during the HM and silicon etch steps and results in increased LER values of 3.7nm in the oxide hard mask. This roughness is partially smoothed along the silicon sidewalls and results in final LER values of 2.8nm into TiN. With the optimized condition in CF_4/CH_2F_2 improved HM LER values of 2.9nm are observed which are partially transferred into TiN.

The fact that changing the HM etch chemistry leads to an improvement of the HM and polysilicon LER supports the assumption done in Section IV.2.2. and suggests that the origin of the silicon LER degradation relies in the HM etch step. However, further investigation should be done to confirm this hypothesis. Besides, although the HM LER was improved from 3.7nm to 2.9nm, the final TiN LER remains similar for any process conditions. In fact, the optimized HM patterning, leads to an improvement of the polysilicon LER at the top of the pattern (LER ~ 2.4nm) which is gradually degraded during the polysilicon process and results in a final TiN LER of 2.7nm. This suggests that the optimization of **the HM etch process does not lead to any further TiN LER improvement.** Further investigation should be done to clarify the origin of this Polysilicon and TiN LER degradation.

IV.3 General conclusion

In this chapter we have studied the photoresist degradation mechanisms in CF_4/CH_2F_2 SiARC etch chemistries.

The photoresists are degraded due to the synergy of the formation of a C-rich FC reactive layer and the strong ion bombardment. Therefore, we have proposed a different SiARC etch process in SF_6/CH_2F_2 chemistries that prevents FC deposition and allows working at lower ion energies. These conditions

allow us to obtain suitable SiARC patterns with a strong improvement of the sidewall roughness (i.e. LER = 2.8nm compared to 10.8nm obtained in CF_4/CH_2F_2 conditions) thanks to the erosion of PR asperities by fluorine induced etching or incidence of grazing ions. Addition of photoresist trim steps also contributes to further reduce the gate sidewall roughness. Thus, reduced SiARC LER values of 2.1nm can be measured after addition of 40s Cl_2/O_2 PR trims steps followed by SiARC etching in SF_6/CH_2F_2 which are not far from the specified LER targets (LER ~1.7nm). Another advantage is that the proposed new process also prevents from wiggling effects even for aggressive gate dimensions. This suggests that the improved gate patterning process is also adapted for the definition of gate patterns for advanced technological nodes where smaller gate CD values are targeted.

However, the gate LER is seen to increase during the HM and Polysilicon etch processes. This LER degradation is suspected to mainly occur during the HM etch process that is carried out in CF_4/CH_2F_2 conditions. Unfortunately, although the modification of the HM etch process does impact the HM and polysilicon LER, it does not lead to any improvement of the final TiN LER. Thus, after full etch process, the best process conditions (with PR trim, SiARC in SF_6/CH_2F_2 and optimized HM opening), result in final LER values of 2.4nm and 2.7nm are measured over Polysilicon and TiN respectively. Therefore, in Chapter V, we will focus on the study of HKMG etch steps and their impact on the final TiN LER.

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Chapter V. LER issue during TiN metal gate etching processes

The previous chapters were dedicated to the impact of cure treatments and HM etch process steps on the final gate LER. In this chapter, a particular attention is paid to the impact of the plasma etch steps involved in the patterning of complex gate stack. So far, most of the studies concerning LER transfer during gate patterning deal with old CMOS generation transistor whose gates are designed with simple stacks composed of polysilicon on SiO_2 oxide gate. The introduction of metal and high-k layers in the gate stack considerably complicates the whole gate patterning process. In fact, specific plasma etch steps need to be introduced to achieve a well defined metal gate pattern. No study has been carried out so far to understand the impact of those plasma steps on the LER transfer. One reason is the metrology limitation to get real information on the TiN LER.
In this chapter, we first present a technique and methodology developed to investigate the TiN roughness. In a second part, the impact of the TiN etch process steps on the gate final LER is studied. Finally, the impact of the TiN film micro-structure on the gate LER is investigated. For this, the TiN film structure is modified by changing the deposition conditions and such films are then tested in real gate integrations.

V.1 Metrology of HKMG Line Edge Roughness

V.1.1 Metrology issue for accurate TiN LER determination

In complex gate stacks, the metallic layer (in our case the TiN film) is very thin and buried under the polysilicon layer as illustrated in Figure V.1.

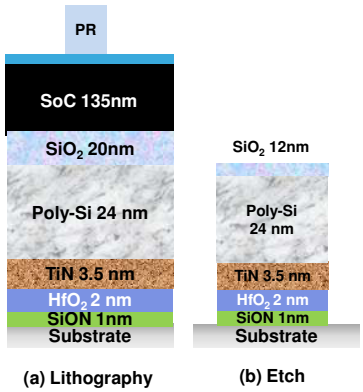


Figure V-1 Schematic representation of 14FDSOI gate stacks after (a) lithography and (b) gate etch steps.

The final gate LER is commonly estimated by CD-SEM after the whole gate process on the stack illustrated in Fig V-1b. CDSEM is a top view observation and it only gives averaged LER information of the whole gate stack. Thus, it is difficult to conclude if the value obtained by CD-SEM is representative of the LER measured at the very bottom of the gate (i.e. in the TiN layer) which is the value directly impacting the electrical performances of devices [1] [2] [3] [4].
Luckily, the tilted AFM metrology technique developed at the laboratory could be a way to evaluate directly the TiN LER. This technique is capable to measure the sidewall roughness along the whole gate stack including the TiN layer. However, the AFM metrology of very thin TiN layers is limited by the small amount of measurement points available in a 3.5nm thick TiN sidewall. To ensure a reliable measure of the TiN layer by AFM technique, thicker TiN layers are needed. Therefore, for all the experiments shown in this chapter, we decided to work over 10nm TiN films. However, it is known that 10nm TiN films may present a different morphology from 3.5nm TiN films. Preliminary results, suggest that 3.5nm TiN films are rougher and probably richer in oxygen than 10nm TiN films. A discussion about the differences observed between 3.5nm and 10nm TiN films is proposed in Annex III.
Moreover, we were interested to see if a methodology could be developed in order to study the TiN LER by CD-SEM. The idea is to remove the HM and polysilicon layers selectively to TiN by wet solutions once the gate has been patterned and to observe directly the TiN pattern using top-down CD-SEM. This methodology is discussed in Section V.1.2 and compared to the AFM metrology.

V.1.2 TiN LER metrology by CD-SEM

V.1.2.1 Substrate preparation for CD-SEM analysis: Choice of wet chemistry

After gate processing, the TiN is buried under the remaining HM layer and polysilicon layers as shown in Fig V-1b. Those layers prevent from a direct estimation of the TiN layer roughness by CD-SEM. Thus we propose to remove those layers using wet chemistries and to subsequently measure the remaining TiN pattern roughness by CD-SEM.

To ensure a successful polysilicon wet removal without damaging TiN layers, a good selectivity towards both TiN and HfO_2 is required.

Silicon is typically etched in a basic solution such as KOH or NH_4OH following an oxido-reduction reaction where silicon is oxidized to form silicates which are then soluble [5]:

$$Si + 2OH^- + 4H_2O \leftrightarrow Si(OH)_2^{++} + 2H_2 + 4OH^- \leftrightarrow SiO_2(OH)_2^{2-} + H_2O$$

Such reactions are known to be selective towards TiN and HfO_2. However, dissolution of thermal silicon oxides (i.e. oxide hard mask) is not efficient in such conditions. This means that, if the NH_4OH solution is applied directly after gate patterning, no efficient polysilicon removal will occur because the remaining SiO_2 hard mask cannot be dissolved in NH_4OH solutions and cannot either be removed by lift-off. Therefore, additional wet chemistries will be required to remove the oxide hard mask.

Oxides are typically etched in HF solutions as shown by the following reaction [6]:

$$SiO_2 + 6HF \leftrightarrow 2H^+ + SiF_6^{2-} + 2H_2O$$

Such reactions can also remove TiN oxides (TiO_x) but are really slow for TiN dissolution and therefore good selectivities can be obtained over polysilicon and TiN [7].

Therefore, the wet chemistry chosen for oxide hard mask and polysilicon removal consists in a two step wet process. First an HF (1%) wet chemistry is applied during 100s to remove the remaining oxide hard mask followed by a NH_4OH (5%) chemistry during 180s for polysilicon removal. This process was developed using a single wafer room.

All the chemical reactions occurring during the wet process with the gate stack materials are also summarized in Table V-1.

Table V-1 Chemical reactions occurring during the HF/NH_4OH wet etch process for polysilicon removal.

Solution	Material	Reaction	Comments
HF	SiO_2	$SiO_2 + 4HF \leftrightarrow SiF_4 + 2H_2O$	Oxides are easily dissolved in HF
	TiO_x	$TiO_2 + HF \leftrightarrow TiF_6^- + 2H^+ + H_2O$	TiO_x is soluble in HF by formation of TiF_6^- anions
NH_4OH	Si	$Si + 2OH^- + 4H_2O \leftrightarrow Si(OH)_2^{++} + 2H_2 + 4OH^-$	Silicon is dissolved in basic solutions by an oxido-reduction reaction
	TiO_x	$TiO_2^+ + 2H_2O \leftrightarrow HTiO_3^- + 3H^+$	Metal oxide passivation layers dissolve in basic solutions by formation of $HTiO_3^-$ HfO_2 or SiO_2 HM solution in NH_4OH is very slow

However, HF wet addition introduces another challenge. In fact, amorphous HfO_2 thin films are known to be soluble in HF [8]. This leads to a lift-off of TiN patterns due to HfO_2 dissolution in HF and silicon bulk etching in subsequent NH_4OH steps (Figure V- 2a). The HfO_2 etch rate in HF strongly decreases with film crystallinity which can be improved either by addition of anneal steps, or by increasing the film thickness at least up to 8nm [8].
Thus, 10nm HfO_2 films previously annealed at 600ºC are used as HK layers. Such HfO_2 films are crystalline and not soluble in HF solution. Therefore, well defined TiN patterns are obtained onto HfO_2 films, that can be measured by CD-SEM to evaluate the TiN final roughness (Figure V-2b).

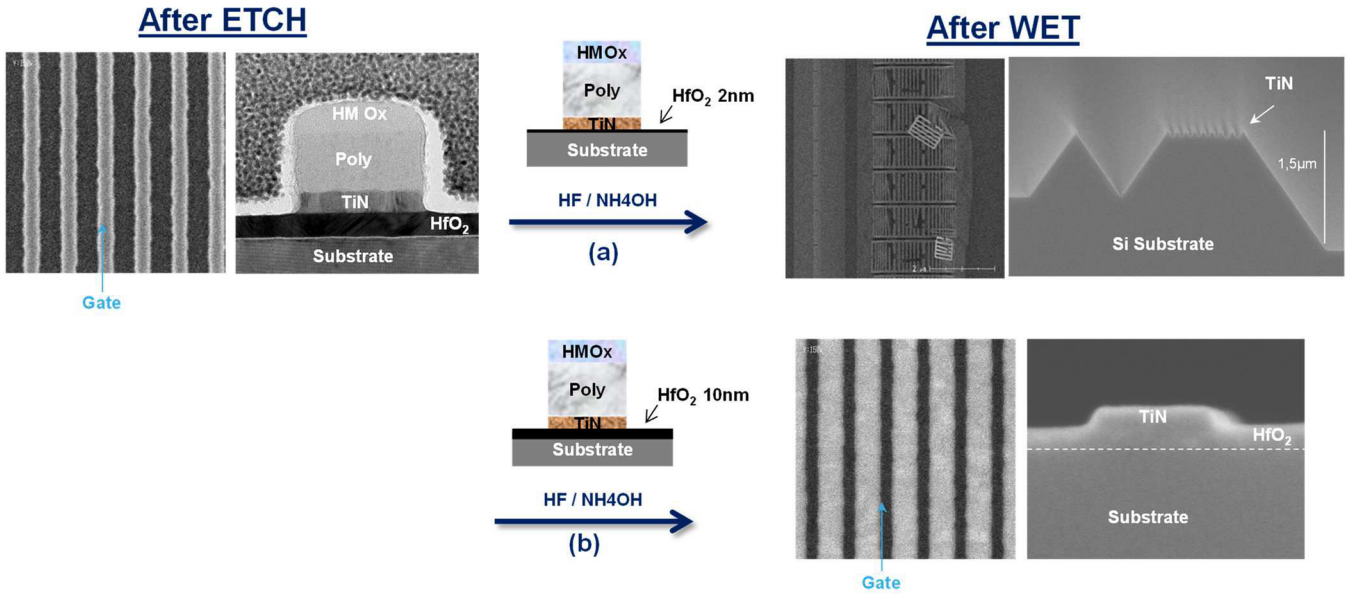


Figure V-2 Gate patterns exposed to the polysilicon wet removal chemistry (HF 1%, NH_4OH 5%). (a) TiN patterns deposed over thin HfO_2 films (2nm) are removed by lift-off due to HfO_2 etch in HF chemistries and subsequent silicon bulk etch in NH_4OH. (b) Increasing the HfO_2 thickness to 10nm promotes HfO_2 crystallization and HfO_2 dissolution in HF solutions is avoided.

In conclusion, the solution that we propose to investigate the TiN layer directly by CD-SEM is to remove the HM/polysilicon by two step wet etch (HF(1%) followed by NH_4OH(5%)). This proposal can work if slight modifications are brought to the gate stack: increase of the TiN and HfO_2 thickness. (c.f. figure V.3)

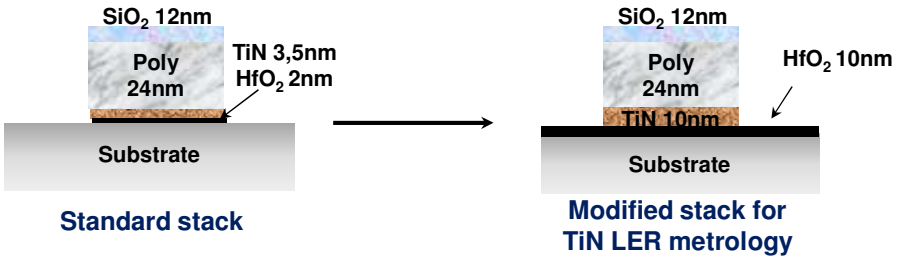


Figure V-3 Schematic representation of the gate stack used for the TiN roughness metrology by CD-SEM

The HF (1%)/NH_4OH (5%) wet chemistry seems a good candidate for polysilicon wet removal. Its efficiency has also been verified by XPS, where no silicon residues were observed over TiN surfaces after wet cleaning. Besides, the impact of the wet chemistry over TiN layers was also analyzed. For this, 10nm TiN layers are deposited on 10nm HfO_2 layers and annealed without any polysilicon deposition at 1000°C for 13s. The surface roughness of such TiN films was measured by AFM before and after exposure to HF/NH_4OH wet chemistries (Figure V-4).

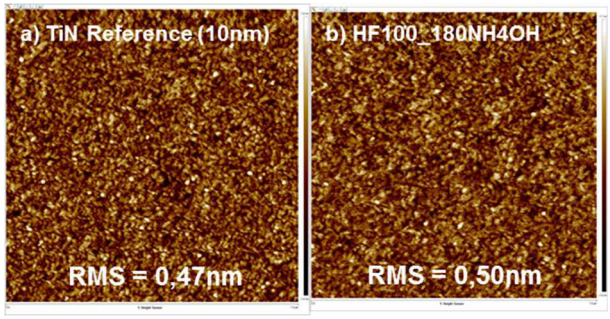


Figure V-4 1x1µm AFM images of TiN films before and after exposure to polysilicon removal wet chemistry in HF (1%)/NH_4OH (5%). Vertical Z scale represents 5nm.

The AFM images of TiN surface before and after exposure to HF/NH_4OH chemistries present a similar roughness of 0.47nm and 0.50nm respectively. The slight increase of the surface roughness can be attributed to dissolution of TiO_x type passivation layers present on TiN surfaces [7]. However, the variation of the TiN surface roughness is not significant and suggests that the HF/NH_4OH chemistry has no impact on the TiN surface roughness and is therefore suitable for polysilicon removal.

V.1.2.2 CD-SEM metrology of TiN layer after etch: comparison to AFM technique

For further verification, the HF/NH_4OH wet chemistry was applied to patterned wafers where the TiN roughness was measured by CD-SEM. The CD-SEM LER values are then compared to LER measured by the AFM technique to evaluate if the CD-SEM metrology is acceptable and representative of the real TiN LER. The CD-SEM and AFM experiments are carried out on the stack described in Figure V- 3.

However, it should be considered that due to the stack modifications, the gate etch recipe was also adapted (i.e. longer TiN etch times) and the CD-SEM metrology was optimized.

The LER measured with both techniques (CD-SEM & AFM) is compared in Figure V-5 for three different cases: No wet (i.e. the HM and polysilicon layers are still in place), and after wet cleaning with two

different HF dilutions for the first wet step (HF 0.5% 100s and HF 1% 100s). The second wet step in NH_4OH remains the same for both samples (NH_4OH 5% 180s).

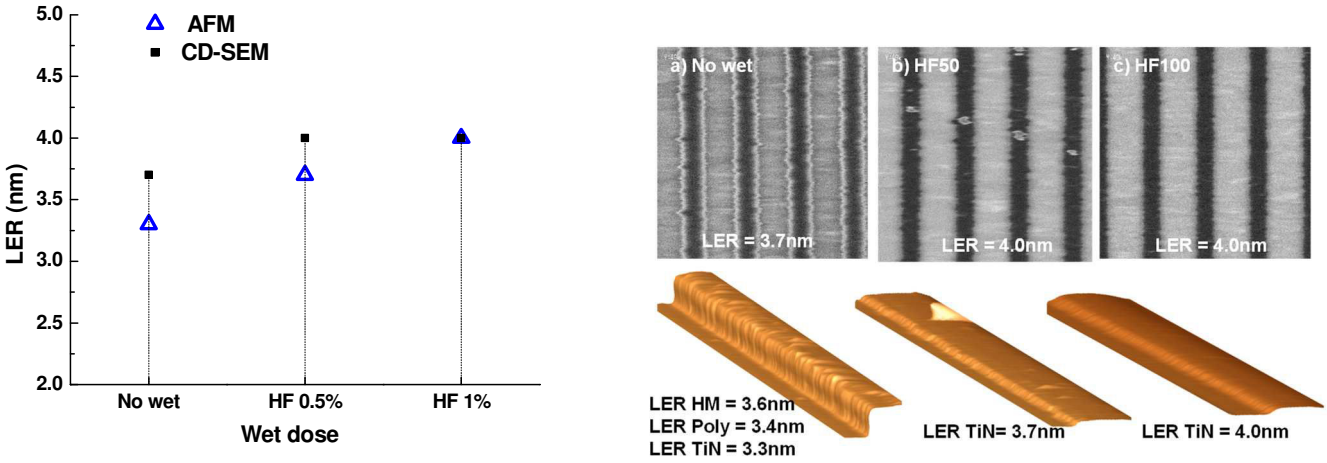


Figure V-5 Comparison of CD-SEM and AFM techniques for TiN LER metrology as a function of the applied HF budget for the first wet step (HF 0.5% 100s and HF 1% 100s), the second wet step remains the same for both cases (NH_4OH 5% 180s). In the case of no wet, HM and polysilicon are still present during the CD-SEM and AFM analyses

If the CD-SEM and AFM LER results are compared, it should be considered that, the CD-SEM metrology consists in a top view roughness metrology while the AFM accounts of the full pattern sidewall roughness. This notion is mainly important concerning the roughness measurements taken over gate patterns where the polysilicon layer remains on top of TiN.

In fact, when **no HF/NH_4OH** wet is applied, the CD-SEM and AFM LER measurements do not agree. The CD-SEM measures a LER of 3.7nm which corresponds to the sidewall roughness measured over the remaining oxide hard mask. In revenge, AFM allows us to measure 3.3nm LER values which correspond to buried TiN layer before wet exposure.

At **low HF budget (HF 0.5% / NH_4OH 5%)** the CD-SEM metrology is disturbed by the non-efficient HM removal at low HF dose as shown in the CD-SEM picture in FigV-5. The remaining polysilicon or oxide HM residues increase the error in the edge detection which gives higher LER values as compared to AFM metrology.

At **higher HF budget (HF 1%/NH_4OH 5%)** both techniques are in a good agreement, and TiN LER values of 4.0nm are measured by CD-SEM and AFM. In this condition, the CD-SEM metrology is considered to be representative of the real TiN roughness.

However, considering only the AFM analysis, a clear evolution of the TiN LER is observed with HF dose, which is attributed to removal of TiO_x passivation layers by the HF solution [7]. These passivation layers are actually removed in the standard gate clean process in HF/HCl solutions that is used after the whole gate plasma patterning (see Chapter I). This means that the LER measured after wet (HF 1% 100s followed by NH4OH 5% 180s) could be representative of the final gate LER in a real process and that the CD-SEM methodology proposed is capable to evaluate the final TiN gate LER after plasma+wet full process.

V.1.2.3 Conclusion

The TiN LER can be successfully measured using the tilted AFM technique. However, to improve the reliability of the AFM metrology, TiN films of 10nm thick are required, which supposes a variation in the film morphology and an increase of the etch process time. Such modifications may impact the TiN roughness but give us an idea of the TiN roughness evolution during the gate etch process. However, the AFM is a slow and not statistic metrology technique that requires particular gate design and wafer cleavage (see Chapter II).

Therefore, we have developed a wet strategy that allows measuring the gate sidewalls roughness directly over TiN by CD-SEM by removing the above HM/polysilicon layers by a wet step (HF 1% 100s followed by NH4OH 5% 180s). The advantage of CD-SEM is that it is an in-line metrology where wafers do not need to be cleaved and that allows measuring the TiN roughness in any structure present within the wafer layout. **However, the proposed methodology requires readapting the gate stack by using thicker TiN and HfO_2 layers. Moreover, because of the dissolution of TiO_x passivation layers during the wet process (section V.1.2.2) the TiN LER values obtained by CDSEM using this methodology are only representative of the TiN LER after the whole gate patterning process, comprising plasma etch steps and wet cleaning.** In this case, AFM and CDSEM metrologies are in good agreement

In the following sections, we have carried out CD-SEM and AFM analyses on the modified gate stack to evaluate the impact of gate etch processes on the TiN LER.

V.2 Impact of TiN etch process to gate stack in final roughness

Addition of metals into the gate stack implies an increased complexity in the development of suitable gate etch recipes. New process steps such as N_2 flash steps and dedicated TiN and high-k etch steps have been added to obtain the desired final gate pattern. Addition of these process steps implies new challenges for the gate etch process. The goal of this section is to evaluate if such steps have an impact on the final gate sidewall roughness.

V.2.1 Process description

The patterning of the high-k metal gate stack (Polysilicon/TiN/HfO_2) requires seven etch process steps as described below:

Polysilicon Main Etch (ME) is achieved in $SF_6/CH_2F_2/N_2$/He plasmas. F neutrals present in the gas phase allow the formation of volatile byproducts such as SiF_4. While the addition of CH_2F_2polymerizing species contributes to polysilicon passivation by line of sight deposition mechanisms that result in the formation of a thin CH_xF_y passivation layer of ~1nm over polysilicon sidewalls (cf. Chapter I) [9].

Polysilicon Over Etch (OE) is achieved in HBr/O_2 chemistries. This process deposits thick SiO_xBr_y passivation layers on the silicon sidewalls that will protect the gate sidewall during TiN and HK etch steps. [10]

An **N_2 flash step** is carried out after polysilicon etching. This step was initially added to further stabilize the silicon sidewall passivation. Besides, the etching ability of N_2 will remove remaining polymer residuals over TiN by formation of CN_x volatile products. [11]

TiN main etch step is based in Cl_2/CH_4 plasma where Cl_2 is the main etchant forming $TiCl_x$ and NCl_x volatile compounds and CH_4 may act as an deoxidizer of TiN surface by formation of CO and CN_x volatile species [12]. **TiN over etch** is also carried out in Cl_2 based plasmas diluted in N_2**.**

The **high-k etch** step in $BCl_3/Cl_2$where B helps to break the Hf-O bonds and increases the HfO_2 etch rate by formation of BO and $HfCl_x$ volatile compounds. [13]

The summary of each step main etch process conditions is shown in Table V-2.

Table V-2 Description of the gate stack etch process conditions

	Chemistry	Power (w)	Bias (V)	Pressure (mT)
Polysilicon ME	SF_6/CH_2F_2	Low	50-100	Low
Polysilicon OE	HBr/O_2	Low	>100	High
N2 flash	N_2	High	No Bias	Medium
TiN ME	CH_4/Cl_2	Low	50-100	Medium
TiN OE	Cl_2/N_2	Low	No Bias	Medium
HK etch	BCl_3/Cl_2	High	No Bias	Medium

V.2.2 Impact of TiN etch process steps onto the gate LER

In this section, we will evaluate the impact of the HKMG etch process steps on the final gate sidewall roughness.

V.2.2.1 Impact of N_2Flash addition

As it has been explained in the previous section, after polysilicon etching in HBr/O_2 plasmas, a continuous $SiOBr_x$ passivation layer is deposited over the whole gate pattern. However, this deposition layer is not stable enough to stand the TiN etching process in CH_4/Cl_2 plasma conditions. As it can be seen in Figure V-6a, previous results obtained at ST Microelectronics show that, polysilicon gates etched without any N_2 flash addition present notched gate profiles at the pattern bottom where the passivation layers become thinner. The addition of N_2 flash step was proposed to improve the quality of the polysilicon passivation layers, and prepare the TiN surface before etching. Thus, polysilicon gates etched with an intermediate N_2 flash steps between the polysilicon over etch in HBr/O_2 and the TiN main etch in CH_4/Cl_2 present straight gate profiles with no notching (Figure V-6b)

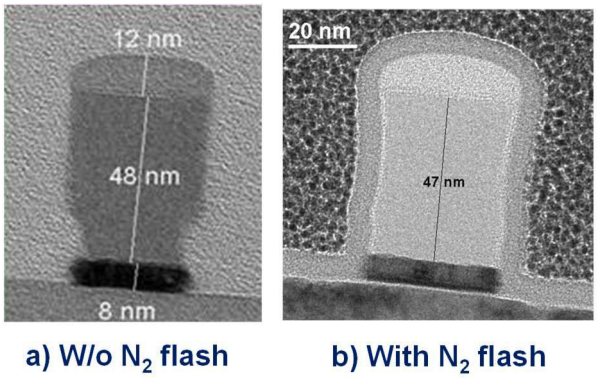


Figure V-6TEM images of High-k Metal gate stacks carried out with and without N_2 flash.

The goal of this section is to verify if the addition of this N_2 flash step has an impact on the gate sidewall roughness. For this, Photoresist gate patterns were transferred into SiARC using SF_6/CH_2F_2 chemistries after previous PR trimming in Cl_2/O_2 chemistries during 40s. The SiARC patterns are then transferred into the gate stack using standards CF_4/CH_2F_2 conditions at 7mT for oxide HM opening. Samples were analyzed after the polysilicon full etching process (ME in $SF_6/CH_2F_2$and OE in HBr/O_2) (Fig V-7a). Then, after a N_2 flash step (Fig V-7b) and finally after the full TiN etch process (ME in CH_4/Cl_2 and OE in Cl_2/N_2) (Fig V-c). TEM images taken after each process step are shown in Figure V-7.

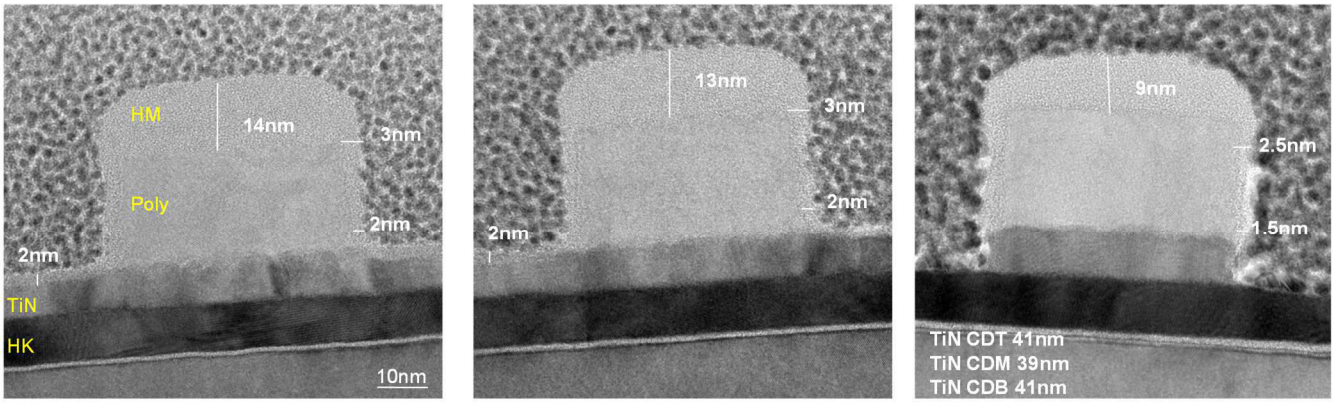


Figure V-7 TEM images of gate stacks after (a) Polysilicon etch, (b) N_2 flash and (c) TiN etch. On TEM images, the measured polysilicon and TiN thicknesses are 20nm and 7nm respectively

After polysilicon etching (Fig V-7a), 14nm oxide HM are left and straight polysilicon profiles are obtained. Presence of a 3-2nm thick passivation layer is observed on polysilicon sidewalls, attributed to the deposition and oxidation of $SiBr_x$ species during the HBr/O_2 over etch step. Besides, the first 2nm of the TiN surface layer seem to be modified, probably due to an oxidation of the TiN surface during the polysilicon over etch step.
After N_2 flash step (Figure V-7b), no particular modification of the gate profile is observed. The passivation layers deposited on polysilicon as well as the modified TiN surface remain untouched.
However, after TiN etching in chlorine based chemistries (Figure V-7c), an erosion of the oxide hard mask and polysilicon passivation layers can be observed. The TiN profile was evaluated by measuring the CD at three different positions, TiN top position (CDT), TiN middle position (CDM) and TiN bottom (CDB). Comparison of the CD evolution along the TiN film thickness illustrates a slight TiN notching of around ~1nm.

The sidewall roughness of each of these samples was analyzed using the tilted AFM technique. The AFM images together with averaged AFM values are shown in Figure V-8. The LER evolution along the pattern height is also shown in Figure V-9. Based on the observations done in the TEM images, the LER curves are shifted vertically for a clearer representation of the LER evolution. It should be considered that due to an error induced by the curvature angle of the AFM tip, the LER measured in the first and last 3nm of the pattern height are not reliable and will not be considered for the LER analysis. It should be noted that since passivation layers are always present on polysilicon (Figure V-7), the obtained LER values do not correspond to polysilicon sidewalls but to the passivation layers.

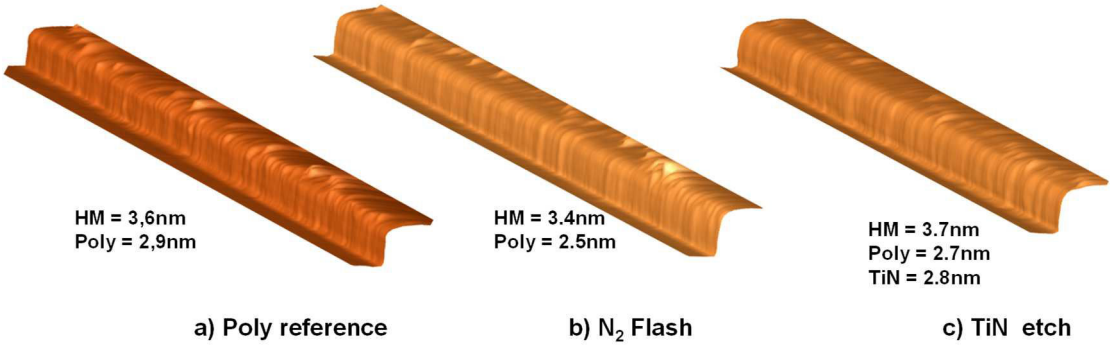


Figure V-8 AFM images and averaged LER values of gate patterns measured after (a) polysilicon etching, (b) N_2 flash and (c) TiN etch.

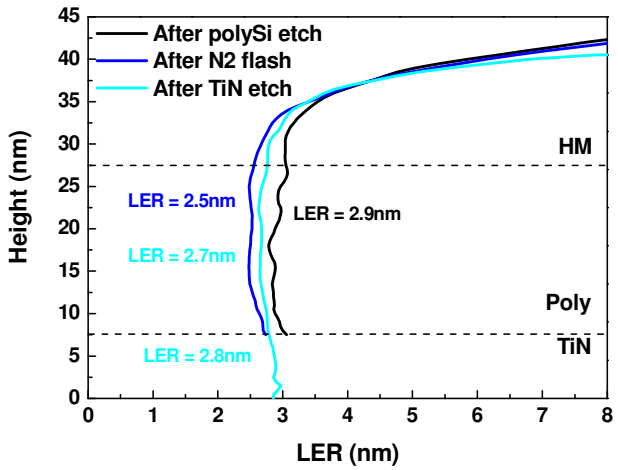


Figure V-9 Evolution of the LER along the pattern sidewalls measured by AFM after polysilicon etching, N_2 flash and TiN etch. The HM/Poly/TiN interfaces are defined according to TEM images. Averaged LER values are also shown for each material. Due to metrology uncertainties, the first and last 3nm of the pattern height are not considered.

After polysilicon etching the silicon sidewalls roughness is uniform along the pattern height and presents an average LER value of 2.9nm. Addition of **N_2 flash** step seems to slightly smooth the polysilicon roughness down to 2.5nm average LER. This smoothening is probably due to a more homogeneous and densified passivation layers formed during N_2 flash step. According to the literature [14], the nitrogen contributes to the halogen removal and substitution of bromine in the $SiOBr_x$ layer to form a denser passivation layer with a SiO_xN_y like composition. This increased nitriding of the passivation layer improves their stability as compared to halogenated layers.
During the **TiN etch process** in chlorine based plasma, the polysilicon sidewall roughness is slightly degraded to 2.7nm which is then transferred into the TiN layer. This roughness degradation is attributed to the erosion of polysilicon sidewall passivation layers.

In conclusion, the addition of N_2 flash step in the gate process leads to the densification of the $SiOBr_x$ passivation layer formed on the polysilicon sidewalls during the polysilicon over-etching, which results in two beneficial consequences for the gate process. First, it protects the polysilicon sidewalls during the TiN etching and prevents from profile distortion (cf. Figure V-6). Secondly, it leads to smoother polysilicon sidewalls (cf. figure V-9). However, the etching of the densified passivation layers during the TiN etch step degrades the polysilicon sidewalls LER.

This degradation is transferred into the TiN layer, masking the smoothening effect of the N_2 flash. Thus, to further improve the TiN LER, TiN etch steps should be improved.

V.2.2.2 Impact of TiN and High-k etch steps on gate LER

In this study, the goal is to further analyze the impact of each of the TiN and HK etch steps on the final gate LER. For this, photoresist patterns were transferred directly into SiARC without any trim addition, using an SF_6/CH_2F_2 SiARC etch condition. Note that, since no trim steps are added, slightly higher LER values will be obtained (refer to Chapter IV) compared to those shown in the previous section (V.2.2.1). Then, the SiARC pattern was transferred into the oxide hard mask with the standard process in CF_4/CH_2F_2 at 7mT. Finally, the gate profile and sidewall roughness were studied after: a) polysilicon etching (ME + OE and Flash N_2), b) TiN ME, c) TiN OE and d) high-k etching processes (Figure V-10). The HK etching process time is the same as in the real process and it is stopped after 2nm HK etching, explaining why the high-k layer is not fully etched in Figure V-10 d).

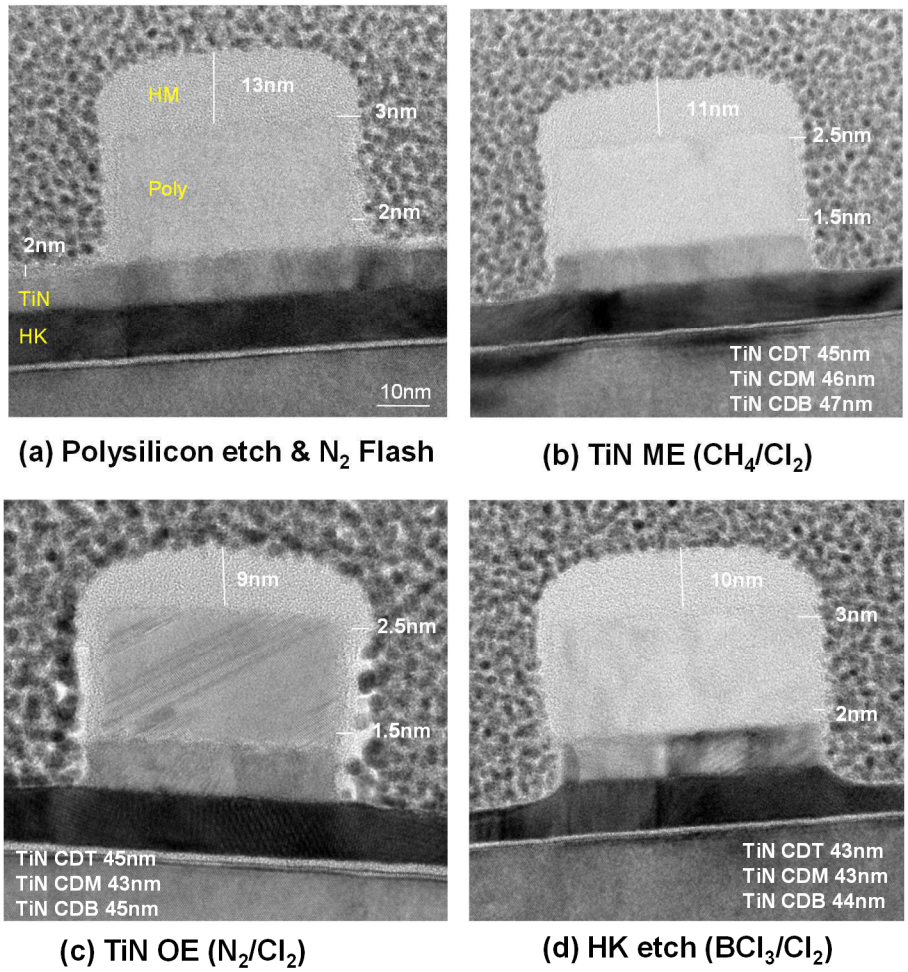


Figure V-10 TEM images of gate patterns after (a) Polysilicon etch and N_2 flash (b) TiN main etch, (c) TiN over etch and (d) High-k etch.

As previously explained, after polysilicon etching, straight gate profiles are obtained. The oxide hard mask is partially eroded, but still 14nm oxide HM is left. Formation of 3-2nm passivation layers is also observed (Fig V-10a).

After the **TiN main etch** in CH_4/Cl_2 plasma, the HM profile as well as the sidewall passivation layers are slightly eroded. Besides, the TiN layer is etched and presents a tapered profile with a CD increase of ~2nm from the top to the bottom (Fig V-10b).
During the **TiN over etch** in Cl_2/N_2, the HM erosion continues (i.e. thickness loss from 11nm to 9nm), though the sidewall passivation layers remain stable and are not further eroded. The TiN profile also evolves from slightly tapered to notched due to lateral etching by Chlorine radicals (Fig V-10c).
Finally, **during the high-k etching** in BCl_3/Cl_2 no erosion of polysilicon passivation layers occurs but instead they seem to become slightly thicker. This is attributed to the formation of non-volatile BCl_x compounds that contribute to the gate sidewall passivation [13]. Besides, the TiN profile is straightened up due to the continuous etching by Chlorine radicals. It should be noted that, to avoid excessive modification of the etch recipe, for this step, the high-k etch process developed for a 2nm HfO_2 layer etching was applied into 10nm HfO_2 layers, which explains why the HfO_2 layer is not completely etched (FigV- 10d).
To study the LER evolution during the TiN and HK etch process, these samples were measured by tilted AFM (Figure V-11). The LER profiles are shifted vertically based on the observations done in TEM images. Figure V-11a shows the evolution of the polysilicon and TiN LER during the TiN etch process (Polysilicon etch, TiN ME, TiN OE and HK etch steps). For an easier interpretation Figure V-11a is zoomed up in Figure V-11b. However, due to the uncertainties in the AFM metrology at the very bottom and very top of analyzed patterns, the HK and HM LER values will not be discussed and only polysilicon and TiN LER evolution is analyzed.

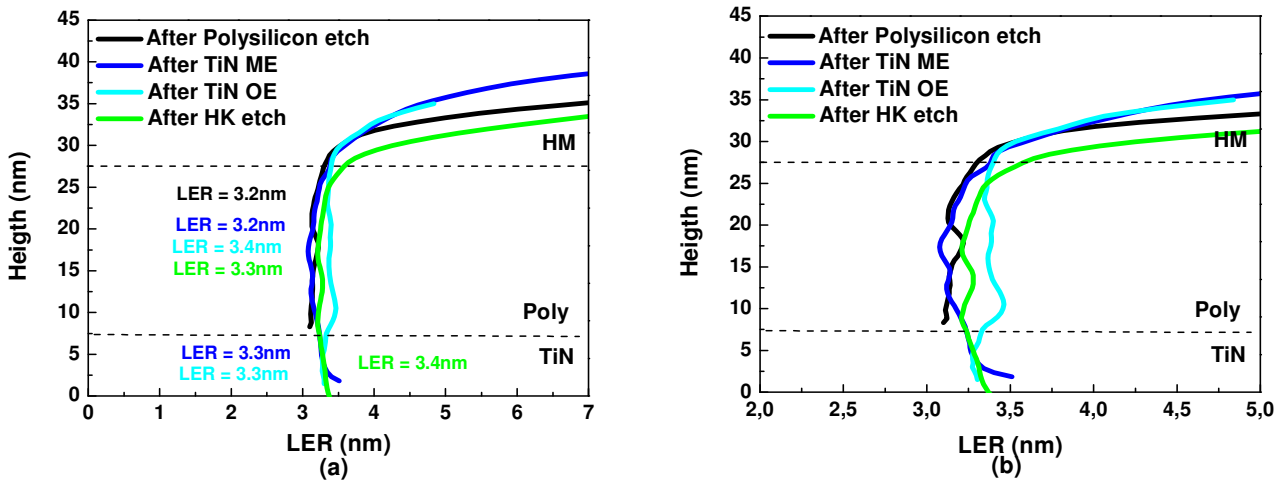


Figure V-11 (a) Evolution of the LER along the pattern sidewalls measured by AFM after polysilicon etch, TiN main etch, TiN over etch and HK etch. A zoomed image is also shown for better understanding (b). The HM/Poly/TiN interfaces are defined according to TEM images. Due to metrology uncertainties, for each sample the first and last 3nm of the pattern height are not considered.

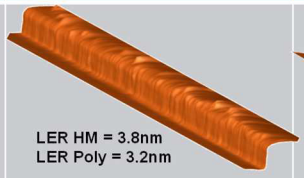
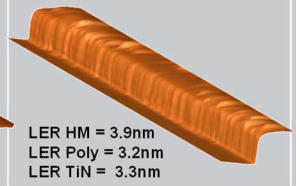
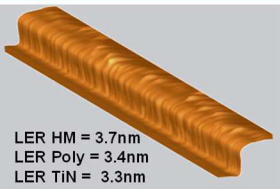
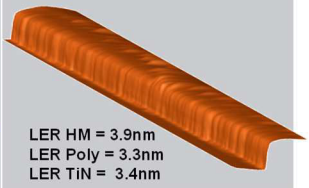
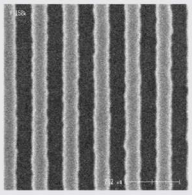
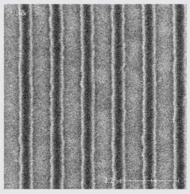
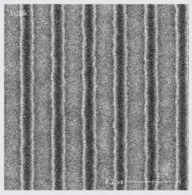
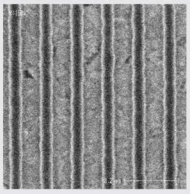
After polysilicon etch, the polysilicon presents a uniform LER of 3.2nm (Figure V-11a), slightly higher than in Figure V-9 where 2.9 nm was obtained since no trim step has been applied here for gate patterning.
After the **TiN main etch in CH_4/Cl_2**, the polysilicon sidewall roughness remains unchanged and is transferred into the TiN layer where an averaged LER value of 3.3nm is obtained (Figure V-11a). This is probably attributed to the high isotropic character of the TiN ME step. In addition, slightly higher LER values are observed at the TiN bottom in Figure V-11b, probably due to TiN pattern footing.

During the **TiN over etch in Cl_2/N_2**, an important LER degradation is observed over the full polysilicon height (Figure V-11a&b). It is probable that a non uniform isotropic radical etching and/or ion sputtering occurs during the TiN OE steps that contributes to the degradation of the LER at the nanometer scale. Even if the sidewall erosion may be too low to be measured over TEM images (Figure V.10.), it may be sufficient to impact the LER and be measured by AFM techniques. The strongest LER degradation is observed at the polysilicon bottom, where the passivation layers are assume to be the thinnest. However this degradation does not impact the Polysilicon/TiN interface. Besides, the isotropic etching of TiN layers does not damage the TiN LER but instead it erodes the TiN footing reducing slightly the TiN LER at the pattern bottom (Fig V-11b).
During the **HK etching process in BCl_3/Cl_2**, the polysilicon LER seem to smooth and recovers a similar LER profile to that measured previously after Polysilicon etch or TiN ME. This smoothening of the polysilicon LER could be attributed to an improved uniformity of the sidewall passivation layers due to the deposition of BCl_x species formed during the HK etch process [13]. The TiN pattern LER remains untouched and equivalent to that measured after TiN OE steps.

From these results we can conclude that the HKMG etch steps impact the Polysilicon LER by sidewall passivation layer reinforcing or etching mechanisms. The TiN LER though, is not modified during process, except from the smoothening of the TiN footing during OE steps. The LER variations observed are really small and can be considered within the error of the AFM metrology. However they could maybe highlight some trends of the LER evolution during the HKMG process.

The results obtained by AFM have been compared to LER measurements done by CD-SEM. For this, the AFM LER is measured over samples directly after plasma processing (i.e. the samples have not seen any wet clean) where the full pattern sidewall is measured and averaged values are calculated for each material. The averaged LER values are then compared to the CD-SEM LER (TableV-3). Concerning the CD-SEM metrology, after polysilicon etching, the CD-SEM LER is measured over HM/Polysilicon gate stacks while after TiN ME, OE and HK etching, CD-SEM LER was measured directly over TiN patterns after polysilicon removal with the two step wet process HF/NH_4OH described in section V.1.2. This means that the LER values obtained over TiN layers after TiN ME, OE and High-k etch by both techniques (CD-SEM and AFM) are not directly comparable since as shown in section V.1.2.2 (cf figure5), the wet process used to remove the HM/polysilicon layers slightly increase the TiN LER.

Table V-3 Averaged LER evolution during the HKMG etch process. AFM values are measured over full gate stacks. CD-SEM values are measured over TiN patterns after polysilicon removal in HF/NH_4OH wet chemistries.

	Polysilicon etch	TiN Main Etch	TiN Over Etch	HK etch
AFM LER *(Full Stack)*	 LER HM = 3.8nm LER Poly = 3.2nm	 LER HM = 3.9nm LER Poly = 3.2nm LER TiN = 3.3nm	 LER HM = 3.7nm LER Poly = 3.4nm LER TiN = 3.3nm	 LER HM = 3.9nm LER Poly = 3.3nm LER TiN = 3.4nm
CD-SEM LER	 4.0nm	 3.5nm	 4.0nm	 3.8nm

It should be noted that CD-SEM is a top view technique and will be therefore representative of the sidewall roughness at the top of the analyzed pattern. Therefore, for the polysilicon reference sample, the measured LER of 4.0nm corresponds to an average LER of remaining HM and polysilicon sidewalls, which is in agreement with the LER value obtained by AFM techniques for the hard mask (3.8nm).

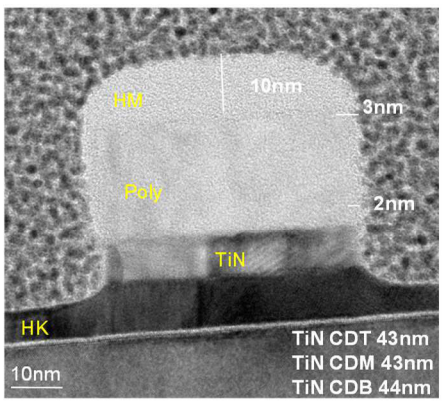
The TiN LER is then measured after TiN ME, OE and HK etch process. According to the AFM results, the TiN averaged LER value does not evolve during the TiN etch process, which suggests that the plasma processing does not impact the TiN LER.

Then, concerning the CD-SEM values, for all samples, slightly higher TiN LER values are obtained compared to those by the AFM. This is certainly because of the HF/NH_4OH wet process applied to the CD-SEM samples which slightly degrades the TiN LER as shown in section V.1.2.2 (Figure V-5).

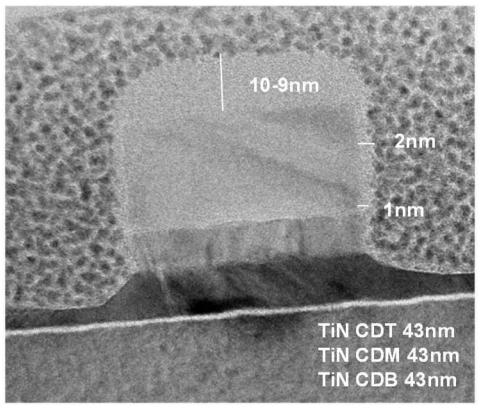
As shown in Table V-3, this degradation is more important after TiN OE and HK etch. This is not surprising because the TiN has been further exposed to plasma after these steps and is probable that the TiN surface reactive layers is richer in chlorine species. This chlorine is replaced by oxygen upon exposure to atmosphere forming more oxidized passivation layers (i.e. TiO_x like) over TiN surfaces after OE and HK steps which will more easily be dissolved by wet solutions. This results in a more important LER degradation after wet conditions observed by CD-SEM and not seen by AFM.

In conclusion, the TiN roughness is not much impacted after plasma processing but the TiN LER can be modified during the wet cleaning steps. Therefore, the TiN LER degradation during gate patterning is a combination of plasma processing (that forms reactive layers which are oxidized under atmosphere) and wet steps (that remove these passivation layers increasing the LER).

To further verify this hypothesis, the fully etched samples were cleaned using a handmade wet process. The cleaning conditions are similar to the HF/HCl wet process carried out at ST after full gate patterning (c.f. Chapter I). Basically, the original process consists in an three step clean process: an O_3 step during 30s for the oxidation of the reactive layers and polymer removal, a hot HCl cleaning step during 150s to dissolve the metallic contamination (La…) and an HF:HCl (1:3) step to remove the remaining metallic oxide passivation layers. To remove the HF residuals, the samples are rinsed with an HCl solution and re-exposed to an O_3 flux. However, in the laboratory, we couldn't carry out the O_3 step or heat the HCl solution. Therefore, the wet chemistry has been slightly modified (i.e. O_3 replaced by H_2O_2) and was carried out at room temperature. TEM images of the etched samples after plasma processing (full etch, including HK etching) and after wet cleaning in HF/HCl solutions are shown in Figure V-12.



(a) Full etch



(b) Wet HF/HCL

Figure V-12TEMimages of etched samples after (a) HK etching and (b) cleaning in HF/HCl solutions

As it can be observed, our modified wet solution in HF/HCl is not very efficient. The HfO_2 layer is partially dissolved in the wet solution; however, the HM and the sidewall passivation layers are not much eroded (i.e. still 2-1nm thick passivation layers remain over polysilicon sidewalls), while the final wet chemistry is aimed to remove all passivation layers and residues. Probably, the H_2O_2 is less efficient than O_3 for the oxidation of reactive layers, and the oxides are less soluble in HCl solutions at room temperature.

Anyway, to determine the impact of the HF/HCl solutions on the TiN sidewall LER, the sidewall roughness of the cleaned samples was measured by the AFM technique. Figure V-13 shows the LER profiles measured after polysilicon etch, full gate etch (including TiN ME, TiN OE and HK etching) and after sample cleaning in HF/HCl solutions.

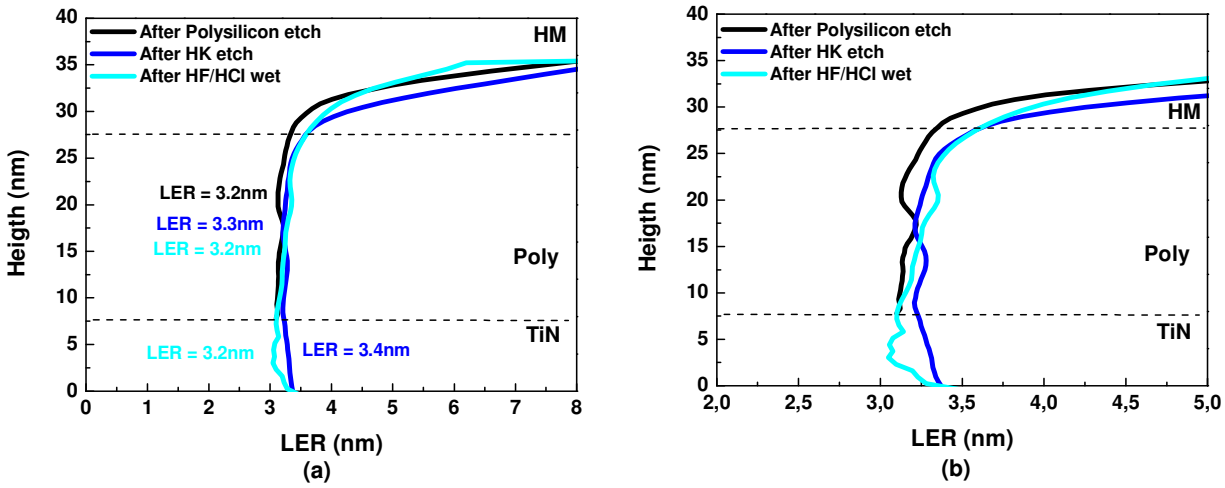


Figure V-13 LER profile evolution after sample cleaning in HF/HCl wet conditions

According to the AFM measurements, the polysilicon sidewall LER is not impacted during the HF/HCl wet step. However, concerning the TiN LER, the HF/HCl solutions seem to smooth the TiN sidewall roughness which is reduced to nearly 3.0nm over the first five nanometers. At the TiN bottom the TiN LER is seen to increase probably due to the presence of the nearby interface with the HK layer.

These results are not in agreement with the results shown in Table V-3, however it should be considered that we are not using the same wet conditions. Apparently, when an HF/NH_4OH is applied, the TiN LER is degraded probably due to the dissolution of the TiO_x passivation layers in the wet solution. In revenge, when HF/HCl solutions are used for the gate cleaning, the TiN LER is smoothed. This may be related to the easier dissolution of metallic oxides in HCl solutions.

It seems that the TiN surface reactive layers formed during plasma processing react differently to different wet chemistries which results in a different LER evolution. Although this experience was only exploratory, it shows that the wet process has a strong impact on the TiN roughness modification. To better conclude, a more detailed study should be carried out to analyze the impact of different wet chemistries on the TiN surfaces previously exposed to plasma processes. However, due to a lack of time, we were unable to explore this approach.

V.2.2.3 Conclusion

In this section we have studied the impact of HKMG etch steps on the TiN sidewall roughness. The HKMG etch process involves, an N_2 flash, TiN ME, TiN OE and HK etch steps.

The N_2 flash step contributes to the densification and smoothening of the polysilicon sidewall passivation layers. However, this smoothening is lost during the TiN etch steps in Chlorine base chemistries due to a polysilicon sidewall etching.

The polysilicon LER degradation mostly occurs during the TiN OE step. However, this degradation does not impact the TiN film which is indeed slightly smoothed due to the TiN foot chopping in Chlorine chemistries.

Though the TiN LER is not degraded during plasma processing, it can be modified during the wet etch processing. Our results suggest that reactive layers formed over TiN surfaces after plasma exposure react with the wet chemistries and impact the TiN LER. Depending on the chemistry of the wet solution, the reactions occurring with the TiN sidewall passivation layers are different and may impact differently the TiN LER.

In conclusion, the metal gate final sidewall roughness results from the contribution of plasma processing and wet cleaning and the wet chemistry plays a key role in the final roughness.

V.3 Impact of TiN deposition parameters

In this section, we will evaluate the influence of the TiN deposition conditions on the final gate sidewall roughness. At STMicroelectronics, the TiN films dedicated for the gate integrations are typically deposited by Radio Frequency Physical Vapor Deposition techniques (RF-PVD). This deposition technique has been detailed in Chapter II. The aim of this section is to modify the TiN microstructure by changing the RF-PVD deposition conditions and evaluate if film granulometry has an impact on the TiN pattern sidewall roughness.

V.3.1 TiN deposition

As described in Chapter II, the most important plasma parameters to modify the TiN film texture are the source RF power, the working pressure and the substrate temperature [15]. The RF power and pressure influence the plasma conditions and the gas ionization (Ar/N_2), and therefore the amount of metal atoms that will be sputtered from the target to reach the film surface. The temperature improves the atom diffusion within the film surface and contributes to the crystal grain formation. In microelectronic applications, there is a constraint to use high substrate temperatures, mostly concerning the high-k materials and metal gate TiN layers [16]. Therefore we preferred to vary the source power and pressure in order to modify the TiN film microstructure and study its impact on the TiN sidewall roughness.

The standard TiN deposition is carried out at 3mT, with an RF source at 600w, a DC at 700w and 20°C. For our study, only one parameter was modified keeping the other conditions constant. However, for confidentiality issues, we are not allowed to give the precise working conditions. The process conditions used are summarized in Table V-4:

Table V-4 TiN RF-PVD deposition conditions

	Film Thickness (nm)	Pressure (mT)	RF (w)	Temp (°C)
RF variation	10	3	**Low, Medium, High**	20
P variation	10	**Low, Medium, High**	600	20

V.3.2 Film characterization

To evaluate the modifications of the TiN film microstructure with deposition conditions, AFM and XRD analysis were carried out over full-sheet wafers.

10nm TiN films were deposited over 10nm HfO_2 films and covered by a 24nm polysilicon layer before annealing. These samples where then annealed and used for the XRD measurements.

The X-ray diffraction technique (XRD) allows us to determine the composition, crystallization degree and crystal orientation of a deposited layer. The principle is based in the fact that crystal grains diffract incidence X-ray light. This scattered light is collected and represented as a peak diffractogram as a function of the scattering angle. Each peak position depends on the primitive cell dimensions of the crystal structure and is therefore representative of the film composition and crystal orientation. By considering the ratios between the integrals of each TiN contribution the preferred crystal orientation can be identified. Besides, the sharpness of the XRD peak is related to the crystal grain size. Thus, sharp XRD diffractograms indicate the formation of densely and uniformly packed crystalline structures. In revenge, broad and not defined XRD peaks are representative of weakly crystallized or nearly amorphous film structures. Thus, each XRD spectrum is unique and representative of a specific material composition. **In our experimental conditions, the XRD beam is irradiated tangent to the sample which allows measuring the TiN horizontal grain size (i.e. Grain width) and lateral film texture (refer to Chapter II) that are those that could impact the CD variation.** Figure V-14 shows the XRD spectra evolution with deposition process conditions.

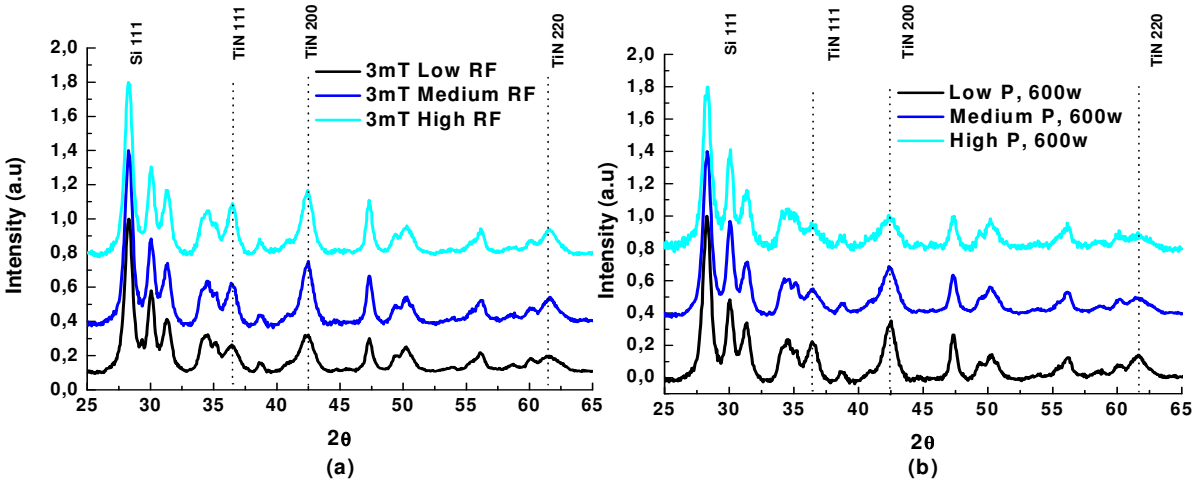


Figure V-14 TiN XRD spectra evolution as a function of the RF-PVD process conditions: (a) source power and (b) pressure. Spectra are taken over 24nm Poly/10nm TiN/10nm HfO2 stacks and are normalized considering the peak intensity of Si [111]. For clarity, a 0.4 shift is applied to each spectrum along the Y axis.

The XRD spectra present many peaks because of the contribution of Polysilicon and crystalline HfO_2 films. For a better comparison, spectra were normalized by the Si [111] peak intensity at $2\theta = 28.24°$

[17] and only the TiN peak contributions are discussed. For clarity, a 0.4 shift is applied to each spectrum along the Y axis.
For each sample, three TiN crystals can be observed which are attributed to the δ-TiN phases with [111] orientation at 2θ=36.46° [18] [19] [20], [200] orientation at 2θ=42.38° [18]and [220] orientation at 2θ=61.48° [18].
As a function of the applied deposition conditions, the TiN XRD spectra are slightly modified.
With increasing source power, TiN peaks are slightly better defined, which suggests an increase in the TiN grain size with increasing source power (Figure V-14a).
At higher working pressures (Fig V-14b), the TiN peaks become broader, sign of the formation of smaller TiN grains.
The TiN grain size evolution as a function of the source power and Pressure increase is shown in Figure V-15.

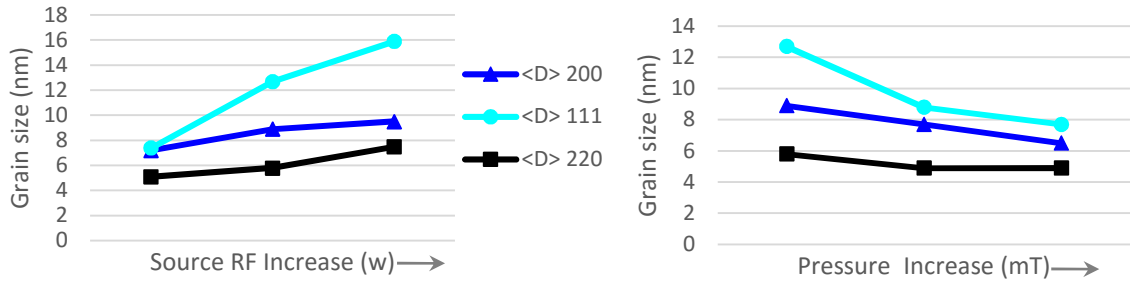


Figure V-15 TiN grain size (<D>) evolution as a function of the applied source power and Pressure for an RF-PVD deposition process

As it can be observed, for any tested condition, the larger TiN grain sizes (16-8nm) correspond to grains with a [111] plane orientation, followed by the [200] orientation (6-9nm) while the crystals orientated in a [220] orientation present the smaller grain sizes (4-6nm). As shown in figure V-15a, the grain size linearly increases with source power. Inversely, the TiN crystal grain size decreases with increasing working pressures (Figure V-15b).

Many studies report that the TiN grain size increases with source power because it results in a larger flux of atoms impinging the film surface and an increase in the energy of each atom. This will increase the amount of nucleation sites but also the diffusion within the film surface, leading to larger grain sizes [21] [22]. Besides, in an early work presented by *Ponon et al* and *Vaz et al*, they stated that TiN films carried out at higher N_2 doses present thicker columnar grains (larger horizontal grain size) [23] [19]. We could imagine that, when high source powers are applied, an enhanced N_2 molecule dissociation occurs that leads to an increased TiN sample nitriding. This increased nitrogen composition on the deposited TiN film may therefore lead to an increase of the horizontal grain size.
The impact of the increased working pressures on the TiN grain size is also well known in the literature [20] [24]. At high working pressures, the mean free path for the atom diffusion within the plasma is reduced. This leads to an increase of the atom collisions within the plasma before reaching the substrate surface. During these collisions, the formation of heavy Ti_xN_y molecules is promoted and an overall loss of the atom kinetic energy occurs. Thus, the TiN particles will arrive at the film surface with few or no energy to diffuse which promotes the formation of nucleation sites, and therefore smaller TiN grains.

However, it should be also considered that when the working pressure is increased, the plasma conditions are also modified. Generally, at higher working pressures, the radical flux is increased. Besides, at equal gas flow, an increase in the working pressure leads to an increase of the particle residence time which promotes plasma-surface reactions that would not occur at lower pressures.

So, in conclusion, working at higher pressures and lower source powers leads to a decrease of the TiN grain size:

- **Smaller TiN grain sizes are obtained for TiN films with lower nitrogen content.**
- **At High P, the molecule mean free path is decreased → small grains**
- **At Low RF, lower film nitriding and lower atom mobility on TiN surface → small grains**

As explained in Chapter I, to improve the electrical performances of the TiN metal gate, TiN films with small grain sizes are preferred [3] [1] [4]. Thus, the TiN deposition conditions with lower grain sizes were chosen to study the TiN roughness evolution as a function of metal gate deposition conditions. The chosen TiN films are the TiN deposited at low source powers (referred as TiN Low RF) and the TiN deposited at high pressures (referred as TiN High P). The TiN deposition conditions chosen for the roughness analysis are summarized in Table V-5:

Table V-5 TiN deposition conditions chosen for TiN film roughness analysis

	Pressure (mT)	RF (w)	Temp (°C)
Standard condition	3	600	20
Low Source Power	3	Low	20
High Pressure	High	600	20

For this study, we are interested in two different roughness values, the TiN surface roughness and the TiN pattern sidewall roughness. The TiN surface roughness gives some insight about the quality of the TiN/Polysilicon interface. In revenge, the TiN sidewall roughness is the responsible of the modifications on the electrical performance of the fabricated devices [2] [4].

V.3.3 Impact of TiN granulometry on TiN surface roughness

The TiN film surface roughness was determined using AFM in a tapping mode. 10nm thick TiN films are deposited with the conditions described in Table V-5. Then, the films are covered by a 24nm polysilicon layer and annealed at 1000°C for 13s. To allow measuring the TiN surface roughness, the polysilicon layer was removed by HF/NH_4OH wet cleaning after anneal.

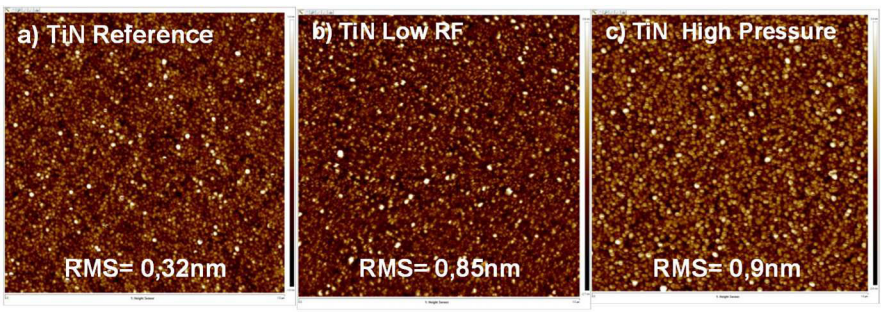


Figure V-16 AFM images of (a) Standard TiN films (3mT, 600w), and TiN films deposited at (b) low source powers and (c) high pressures. Images are taken after polysilicon removal by HF/NH_4OH wet solutions. The z vertical scale is 8nm.

As shown in Figure V-16, the standard deposition condition at 3mT and 600w source presents the lowest surface roughness of 0.32nm. The TiN films deposited at lower RF power or at higher working pressure present similar surface roughness of 0.85nm and 0.9nm respectively.
The XRD and AFM results obtained for these three samples are summarized in Figure V-17:

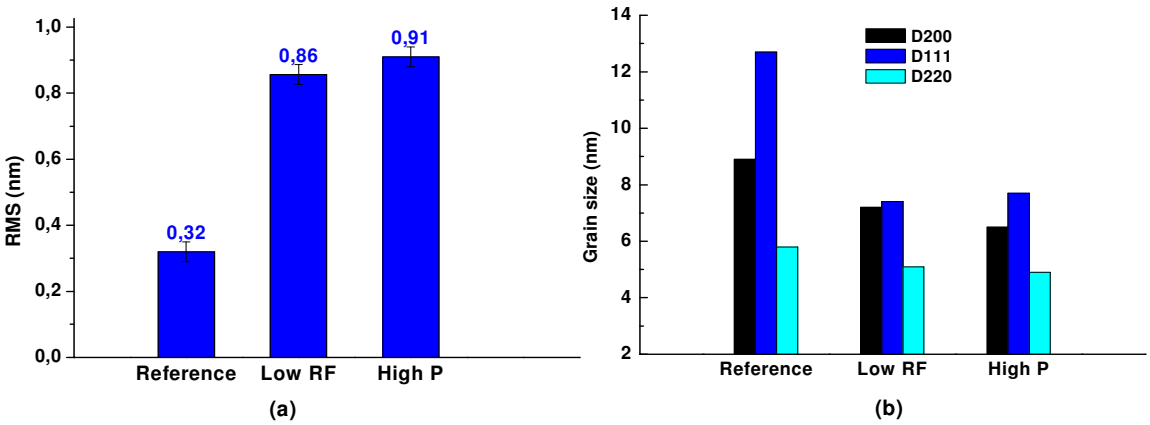


Figure V-17 (a) Surface roughness (RMS) and (b) horizontal grain size of standard TiN films and TiN films deposited either at Low RF or at High Pressure determined by XRD

The TiN films carried out at low source powers (Low RF) or high working pressures (High P) present a really similar microstructure in terms of horizontal grain size, and surface roughness. In both cases, smaller TiN grains and rougher TiN surfaces are observed.

Though the TiN surface roughness was not improved by modulating the RF-PVD deposition conditions, the film surface roughness may not be related to the TiN sidewall roughness after plasma etching.

V.3.4 Impact of TiN granulometry on TiN sidewall roughness (LER)

To study the evolution of the TiN sidewall roughness for TiN films with different microstructures, such TiN films were integrated into full gate stacks and etched following the same process conditions. Thus the TiN main etch (ME) was carried out in CH_4/Cl_2 chemistries for 9s and followed by a TiN over etch (OE) in Cl_2/N_2 chemistries during 18s. The TiN etch process was monitored using the optical emission intensities of the CN and CO at 387cm^{-1} and 520cm^{-1}and the Light Signal Reflectometry (LSR). The followed ray varies from 260-267nm depending on the TiN film. The TiN etch endpoint followed by the LSR signal is shown in Figure V-18.

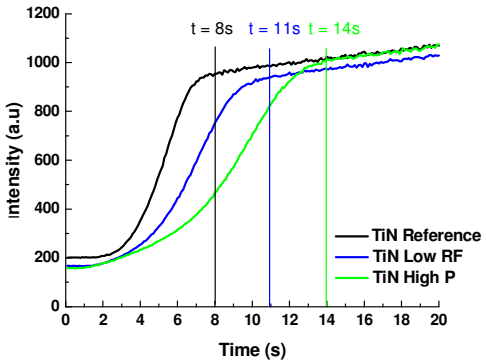


Figure V-18 LSR signal evolution during the TiN main etch process in Cl_2/CH_4. The followed ray varies from 260-267nm depending on the TiN film.

According to the optical emission traces and the LSR, an etch rate of 1.2nm/s was estimated for standard TiN while etch rates of 0.9nm/s and 0.7nm/s are measured for TiN films deposited at low source powers (Low RF) and TiN films deposed at high pressures (High P), respectively. Since all the TiN layers integrated in the gate stack were exposed to the same total process time (9s ME + 18s OE), the differences in the TiN etch rate result in lower over etch times particularly for TiN films deposited at High Pressures.

The gate profiles obtained for different TiN films are shown in Figure V-19. To facilitate the observation of the TiN grains, zoomed images of the TiN profile with stronger contrast are also shown.

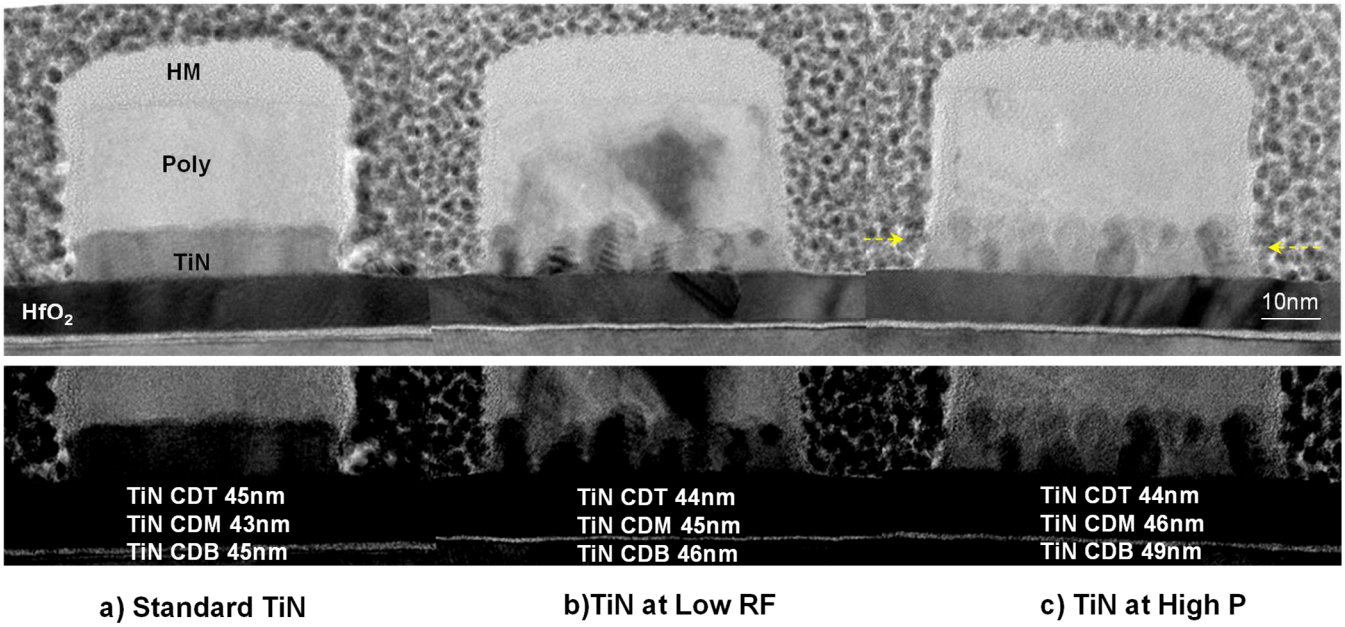


Figure V-19 Full etch TEM images of gate stacks with different TiN layers (Standard TiN, TiN Low RF and TiN High P). Zoomed images of the TiN film with stronger contrast are also shown. For High Pressure TiN films a double TiN layer is observed. Arrows are added to guide the eyes.

Concerning the gate profile, since the same etch conditions was used for the three samples, the polysilicon profiles are relatively similar. The remaining HM thickness varies between 8-10nm probably due to a variation on the deposited oxide thickness during the gate stack elaboration. The polysilicon sidewall passivation is also equivalent for the three samples and varies between 2.5-1.5nm from the top to the bottom of the gate profile.

Concerning the TiN, it can be observed that the TiN films deposited at Low RF and those deposited at High P present a non-uniform polysilicon/TiN interface as compared to the smooth interface observed for standard TiN. This increased interface distortion is attributed to the stronger surface roughness of 0.8-0.9nm measured over Low RF and High P TiN films while only 0.3nm were measured over reference TiN (cf Figure V-16).

The TiN profile and grain structure also differ from one sample to the other. Considering that the same TiN etch process was used for the three samples, the differences in the TiN profile are attributed to differences in the TiN etch rates.

In standard TiN films (Fig V19a), the film granulometry seems quite uniform. The TiN profile shows a slight notched profile probably due to excessive over etching.

Concerning the TiN film deposed at Low RF, an irregular grain distribution is observed (Fig V-19b). However, TiN grains seem to be vertical in a columnar like fashion and cover the whole film thickness. The TiN profile is also straighten up and no TiN notching is observed which is in a good agreement with

the lower TiN etch rates measured for these samples (i.e. less lateral erosion during the shorter over etch process).
Finally, TiN films deposed at high pressures (Fig V-19c) present remarkable tapered profiles where the TiN CD is increased of ~4nm from the top to the bottom. This increased tapered profile is attributed to the low TiN etch rates and therefore, the reduced TiN over etch step. The TiN grains also present a different distribution. According to the TEM images, they seem to be smaller and they do not grow all along the full film thickness. In a certain manner, we could imagine the formation of an interface around the middle of the TiN film (Arrows are added to guide the eyes).

The origin of this particular crystal structure is still unknown. *Goullet et al* studied the TiO_2 film growth at low pressures (3mT) and quite low substrate temperatures (<100°C) as a function of the applied substrate bias [25]. In their experiments, they observed a gradient on the TiO_2 crystalline structure that led to the formation of a two layer system. The film bottom consists in a dense and ordered TiO_2 layer while the top layer is formed of an unordered TiO_2 layer with lower film densities. This bi-layer model was mainly observed for samples processed with no or little applied bias and is assume to be reduced due to the increased film densification at high bias voltages [25].
Another hypothesis was presented by *Ohya et al* who have studied the deposition of TiN films as a function of the working pressure (2-9mTorr) at room temperatures (25ºC) [24]. According to their studies, increasing the working pressure during the TiN films deposition process leads to the formation of clearer grain boundaries and increases the levels of sample oxygen and carbon contamination [24]. In fact, the oxygen segregates through the grain boundaries where it forms oxide layers that block particle motion and interrupts grain growth [26]. Since the grain formation is dependent on the number of mobile grain boundaries [27], we could image that stronger oxygen diffusion at high pressures could modify the grain formation and lead to smaller grains with a less columnar structure.

Thus, an increase of the oxygen diffusion (after deposition) seems to be the most probable contributor for the TiN film modification at high pressures. Besides, an increased oxygen content on TiN films deposited at High Pressure could also explain the lower etch rate observed in CH_4/Cl_2 plasmas for High P TiN films due to the higher dissociation energy of Ti-O bonds (666 KJ/mol) as compared to Ti-N bonds (476 KJ/mol) [28].

To determine if the evolution of the TiN film morphology has an impact on the sidewall roughness, the three gate patterns were measured by tilted AFM. The interfaces between HM/Polysilicon/TiN layers are drawn according to the TEM images shown in Figure V-19. Due to the uncertainty of the AFM metrology the first and last 3nm of the gate profiles are not considered for the roughness analysis.

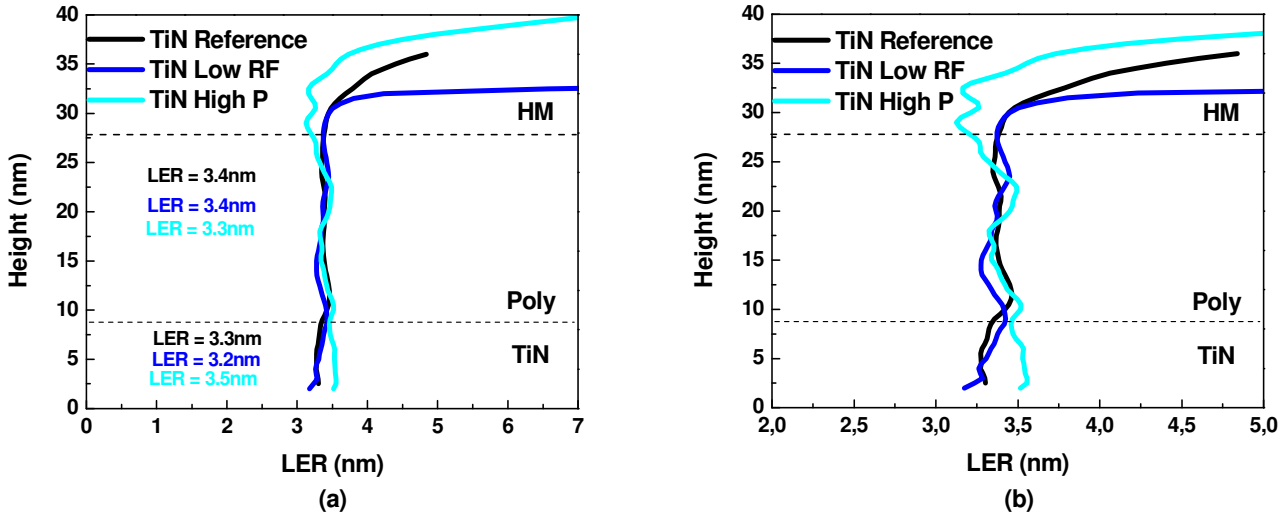


Figure V-20 (a) LER evolution along the pattern height measured by AFM after full etch. Different TiN films are compared, the standard TiN, TiN Low RF and TiN High P. (b) Zoom up representation of the LER evolution shown in (a). The HM/Poly/TiN interfaces are defined according to TEM images. Due to metrology uncertainties, the first and last for each sample 3nm are not considered.

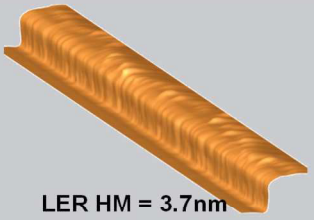
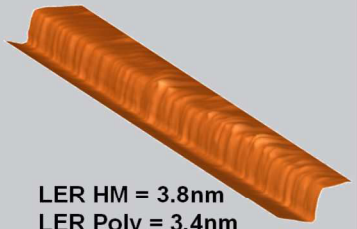
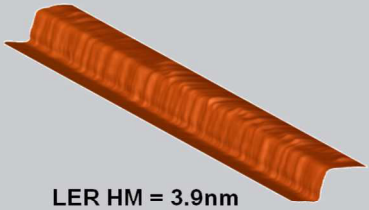
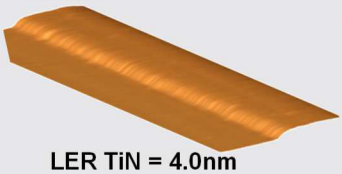
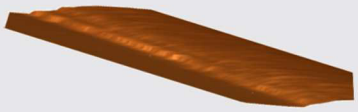
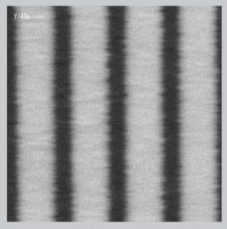
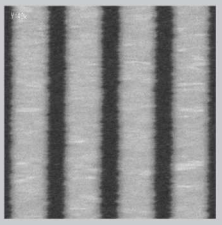
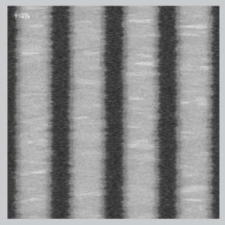
Concerning the polysilicon layer (Fig-V20a), as expected, all three samples present the same LER profile, as all of them were etched using the same Polysilicon/TiN etch recipe.
Now, concerning the TiN sidewall roughness, the standard TiN and the TiN deposed at Low RF power present similar LER profiles. In revenge, rougher LER profiles were measured for TiN layers deposed at High P (Figure V-20 a&b).
According to the differences in the TiN film microstructure (Section V.3.1.a), we could expect to obtain a similar LER for Low RF and High P TiN patterns which will be different from that of standard TiN. However, the obtained results suggest that the differences in the TiN film microstructure do not lead to major changes in the sidewall LER.
Concerning the High P TiN patterns, the increase of the TiN sidewall roughness can be attributed to the lower etch rates measured over High P TiN films (0.7nm/s vs. 1.2nm/s for reference TiN). In fact, since the same TiN etch process time was used for the three samples (ME 9s + OE 18s), a lower TiN etch rate results in a lower OE for High P TiN patterns. In section V.2 we proposed that the TiN OE contributes to the TiN foot smoothening, and may improve the TiN sidewall roughness.

Therefore, we suppose that the reduced OE for TiN patterns carried out at High P, leads to the formation of stronger TiN footing and to the increase of the TiN sidewall roughness.

To better conclude, it would have been interesting to study the TiN LER evolution as a function of the OE time and verify if the High P TiN roughness is smoothed with increasing OE time. However, due to a lack of time, this approach was not studied.

The averaged LER values obtained by AFM for each material were also compared to CD-SEM LER measurements done over dense line patterns. However, it should be considered that for CD-SEM metrology, TiN LER is measured over cleaned TiN patterns where the polysilicon layer has been removed by HF/NH_4OH wet cleaning. To better compare the TiN LER obtained by AFM and CD-SEM before and after cleaning, the cleaned TiN samples were also measured by AFM. All the results are summarized in Table V-6.

Table V-6 Averaged AFM LER values of Standard, Low RF and High P TiN films after full etch and after wet poly removal. CD-SEM values are measured over TiN patterns after polysilicon removal in HF/NH_4OH wet chemistries.

	Std TiN	TiN Low RF	TiN High P
AFM LER *(Full Stack)*	 LER HM = 3.7nm LER Poly = 3.4nm LER TiN = 3.3nm	 LER HM = 3.8nm LER Poly = 3.4nm LER TiN = 3.2nm	 LER HM = 3.9nm LER Poly = 3.3nm LER TiN = 3.5nm
AFM LER *(after clean)*	 LER TiN = 4.0nm	 LER TiN = 3.8nm	 LER TiN = 5.2nm
CD-SEM LER	 4.0nm	 3.9nm	 4.7nm

The AFM LER values measured on cleaned TiN are equivalent to CD-SEM LER and higher than LER measured over full stack samples. These results confirm that both techniques are in a good agreement and that the HF/NH_4OH wet removes TiO_x passivation layers and therefore impact the TiN sidewall LER.

The reference TiN and the Low RF TiN present a similar LER of 3.3nm after etch, which is increased to ~4nm after wet cleaning. The High P TiN presents a slightly higher LER of 3.5nm after etch. However, after wet cleaning, the LER is strongly degraded and higher LER values are measured by AFM (5.2nm) and CD-SEM (4.7 nm) as compared to the 4.0nm measured over reference and Low RF TiN patterns.

This increase on the TiN roughness is attributed to a further degradation of the High P TiN in HF/NH_4OH solutions. If the High P TiN film is richer in oxygen as we suspect, it is not surprising that it is further degraded in HF/NH_4OH solutions due to the dissolution of TiO_x species.

These results suggest that, the wet solutions impact differently the TiN LER depending on their composition (i.e. oxygen content) while the TiN microstructure has no relevant impact on the TiN LER.

V.3.5 Conclusion

The TiN microstructure and its physico-chemical properties can be modified by changing the RF-PVD deposition conditions.
The film microstructure, such as grain size and the TiN surface roughness, has an impact in the quality of the polysilicon/TiN interface. Thus, 10nm TiN films with smaller horizontal grains sizes but stronger surface roughness lead to irregular Poly/TiN interfaces. However, the TiN film granulometry has no strong impact on the TiN sidewall roughness.
In revenge, the TiN physico-chemical properties influence the TiN etch rates; either in dry or in wet processes. This implies that depending on the film composition, some TiN films will be more sensitive to the wet cleaning processes and may result in different LER values.

From these results we conclude that, by changing the TiN film deposition conditions, the film composition and the metal gate final roughness can be modified. Therefore the LER can be improved by modifying the TiN RF-PVD deposition conditions.

V.4 General Conclusion

In this chapter we have studied the impact of HKMG etch processes in the final gate LWR. According to our observations, the TiN final roughness results from the contribution of plasma processing and wet cleaning steps. The TiN LER is not largely modified during plasma processing, however, it is strongly impacted during the wet cleaning process. This is suspected to occur due to the dissolution of TiN passivation layers deposited over TiN sidewalls during plasma processing. Depending on the composition of the TiN passivation layers, and the wet chemistry solution, the TiN LER modification may vary.

In addition, we have shown that the TiN grain size has no or little impact on the TiN LER. In revenge, the TiN chemical composition, and more particularly the TiN oxygen content has an impact on the TiN LER. Further oxidized TiN films seem to be more sensitive to HF/NH_4OH solutions and are degraded during the final wet steps.

The wet processing seems to have a capital role on the TiN final roughness. However, due to a lack of time we could not further investigate this approach.

Finally, it should be noted that our experiments were carried out over 10nm TiN films which may differ from the 3.5nm TiN films used in real gate integrations. It seems that 3.5 and 10nm thick films do not exactly present the same microstructures and chemical composition (Annex III). 10nm thick TiN layers present larger horizontal grain sizes and are richer in nitrogen and poorer in oxygen than 3.5nm thick TiN films. According to section V.3 the grain size has no impact on the TiN sidewalls roughness after etching. However the surface roughness and also the sidewall roughness are stronger for TiN films that are richer in oxygen (such as 3.5nm thick TiN layers). The further oxidized TiN films are more impacted by wet cleaning steps and result in higher surface and sidewall roughness. Even if not verified, we suspect that the 3.5nm thick TiN will be rougher after the wet process than the 10nm thick TiN.

In a future work, it would have been interesting to study if the same results are obtained for other TiN deposition techniques. For example, TiN PE-ALD deposition is a promising technique that allows deposing dense TiN layers with improved film uniformity. It could be interesting to determine if increased film uniformity leads to improved TiN sidewall roughness.

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General Conclusion

It is well know that the dimensional control is one of the main issues concerning the gate patterning. The dimensional control includes the CD control (intra-wafer, inter-wafer and inter-lot) and the dimensional control over smaller scales considering the CD variations over one same gate feature, also called, the Line Edge Roughness (LER). Along with downscaling, the specifications concerning the dimensional control become more and more restricted. This is particularly challenging for the latest CMOS technologies, such as, the 14FDSOI where, numerous plasma etching steps are involved in the high-k/metal gate patterning, each of them being a source of variability.

Thus, the main goal of this PhD work was to evaluate the impact of gate patterning processes on both the dimensional control and LER of a 14FDSOI gate pattern. This work was particularly dedicated to the understanding of the gate pattern deformations during the etch processes and the LER evolution all along a gate stack including the HKMG ultra-thin layers.

At first, we were interested in studying the impact of HBr plasma cure step on 14FDSOI gate integrations where complicated 2D patterns are defined. In fact, cure steps were established as post-lithography treatments to increase photo-resist stability and to improve LER and CDU before pattern transfer. However, we have highlighted that, for the latest 193nm photoresist platforms, the cure step leads to resist flowing phenomenon. This resist flowing is dependent on the photoresist and when it is observed in 2D gate patterns it results in what is called the gate shifting phenomenon; namely, a misplacement of the gate pattern that results in a bad gate to contact alignment and leads to a loss of the electrical performance. We have shown that the VUV irradiation emitted by HBr plasma is responsible for the resist flowing. Thus, to limit the gate shifting we have proposed optimized cure conditions with limited VUV irradiation. However, while low VUV dose during plasma treatments is required for limiting gate shifting, high VUV dose is mandatory to harden the photoresist pattern and prevent from resist LWR degradation during SiARC etching. A compromise needs to be found to limit the pattern deformation while preserving suitable pattern LER. As the gate shifting is the key issue for the 14FDSOI technology, the strategy adopted was to introduce resist pretreatments with low VUV dose, such as resist trimming in order to limit the resist reflow, and thus gate shifting. The consequence is that the SiARC etch step needs to be revisited to improve overall pattern transfer.

Thus, in a second part of this work, we decided to study the masking strategies and more particularly, the photoresist degradation mechanisms in the state-of-art SiARC etch chemistries based in CF_4 plasmas. As it was observed, the photoresists are degraded due to the synergy of C-rich fluorocarbon reactive layer formation and the energetic ion bombardment. To limit the photoresist degradation, we proposed a different SiARC etch process in SF_6/CH_2F_2 chemistries that prevents FC

deposition and allows working at lower ion energies. This conditions allow to obtain suitable SiARC patterns with controlled sidewall roughness thanks to the erosion of PR asperities by fluorine induced etching or incidence of grazing ions. With this optimized SiARC process (Trim + SiARC etch in SF_6/CH_2F_2), the gate shifting value is not degraded and remains as low as 0.5nm with an improved sidewall roughness of LER = 2.1nm compared to the standard process (Cure + SiARC etch in CF_4/CH_2F_2), where gate shifting values of ~6nm are obtained with a sidewall LER of 2.5nm. We have then studied the transfer of the roughness during the patterning of the hard mask and polysilicon layers and showed that the gate shifting is maintained to low values during the transfer but the line edge roughness is slightly degraded (LER = 3.3nm measured on Silicon). We suspect that the HM opening plasma step is responsible for this LER increase but we did not succeed in improving the process.

Finally, the last part of this work was dedicated to the study of the LER during the patterning of the metal/high-k layers composing the 14FDSOI gate stack. More particularly, the study was focused on the impact of HKMG etch steps on the metal gate's final roughness (TiN). For this, we used a new metrology technique elaborated in our laboratory, the Tilted AFM technique. This technique allows us to scan with an AFM probe, the sidewalls of a full gate stack including the buried TiN layer. Besides, we also wanted to establish a new methodology to be able to measure the TiN LER by standard CD-SEM techniques. This strategy consists in removing the HM and polysilicon layers using wet solutions and leaving the TiN pattern untouched. The wet solutions probably dissolve the TiN sidewall passivation layers and therefore this technique is representative of the HKMG sidewall roughness after full patterning process including the gate cleaning wet steps. By comparing both techniques (AFM and CD-SEM), we can determine the impact of dry and wet etch processes on the TiN sidewall roughness.

From this study, we conclude that the TiN roughness is not largely modified during plasma processing; however, it is strongly modified during the wet cleaning process. This modification results from the dissolution of TiN sidewall passivation layers that are formed during plasma processing. Depending on the chosen wet chemistry, the impact on the TiN LER may vary. This suggests that the wet processing has an important role on the TiN roughening mechanisms. Besides, we were also interested on the impact of the TiN granulometry on the HKMG sidewall roughness. According to our results, the TiN grain size has no or little impact on the TiN LER. In revenge, the TiN chemical composition, and more particularly the TiN oxygen content has an impact on the TiN LER. Further oxidized TiN films are more sensitive to wet solutions and are degraded during the final wet steps. Finally, it should be noted that our experiments were carried out over 10nm TiN films which may differ from the 3.5nm TiN films used in real gate integrations. Even if not verified, we suspect that the 3.5nm thick TiN will be rougher after the wet process than the 10nm thick TiN.

During this PhD work we have seen the main challenges for the improvement of the CD control in 14FDSOI gate patterns. We have developed a new gate patterning process (with PR trimming and SiARC opening in SF_6/CH_2F_2 and optimized HM etch process) that allows the definition of 14nm gate patterns without pattern deformations and with suitable LER values. The gate shifting was reduced from 6nm down to 0.5nm and the polysilicon LER was improved from 3.3nm to 2.7nm. The specifications point that for 14FDSOI integrations, gate patterns should be defined with a gate shifting not higher than 1nm and a maximum LER 1.7nm (LWR = 2.4nm). According to our results, the developed process condition is suitable even for very small gate patterns, which reveals that it could be also suitable for gate patterning for advanced technologies, but still remains far from the defined specifications (LER = 1.7nm). The proposed new process has been implemented at STMicroelectronics and is being tested over a certain number of different products. In addition, we have shown that the interactions between

the different patterning stages, including, lithography, etch and wet steps become very important and can even be limiting in terms of CD and LER control. Combined efforts need to be done in order to develop gate patterning processes that satisfy the CD control specifications.

For a future work, it would be interesting to further study the photoresist reflowing phenomenon for different photoresist platforms. A more detailed comprehension of the physico-chemical polymer modifications during plasma processing is required in order to develop more suitable resist platforms. In addition, we outlined the fact that the LER increases during the HM etch steps in CF_4/CH_2F_2. Further studying of this approach is also important to find new methods to further improve the gate LER all along the gate etch process. Finally, we also highlighted the strong impact of TiN deposition conditions and subsequent wet steps on the TiN LER modification. To further understand these LER modifications, it would be necessary to carry out a more detailed analysis of the TiN composition as a function of the deposition conditions and study the impact of the TiN composition on the dry and wet etch mechanisms. A comparison of the results obtained on RF-PVD TiN layers with TiN films deposed using other deposition techniques, such as PE-ALD, would be interesting to determine if different metal deposition conditions may impact the gate final roughness.

Annex I
Deposition of TiN films by RF Physical Vapor Deposition (RF-PVD)

In a PVD deposition process, the thin film layer growth occurs in three steps. First, the sputtered atoms reach the substrate surface. In a second step, the sputtered atoms are adsorbed onto the substrate surface. Depending on the available thermal energy, these atoms will diffuse within the substrate and are resembled to form nucleation sites. In a third step, the atoms move within the coating film towards their final position, process known as "bulk diffusion". In this last step, the nucleation sites grow and form the crystal grains that are observed afterwards in the deposited films [1].

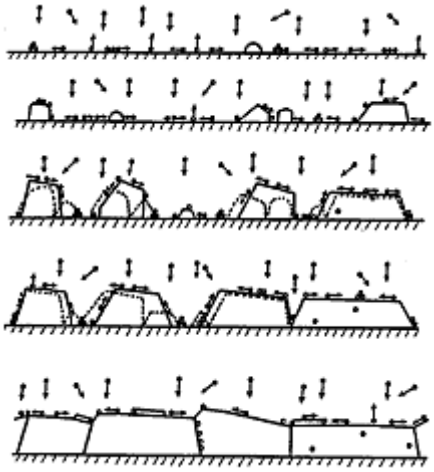

Figure 1. .Schematic diagram illustrating fundamental growth processes controlling micro-structural evolution of PVD deposited films: Nucleation, island growth, coalescence of islands, grain coarsening, and the development of continuous structures and film growth [2].

The grain size therefore depends on the atom transport (or the amount of atoms impinging the substrate surface) and the atom diffusion. The atom transport is typically controlled by the working pressure or reactor geometry (distance between both electrodes). In revenge, the atom diffusion is mostly controlled by the substrate temperature, surface conditions (i.e. substrate roughness) and can be also influenced by energetic particle bombardment. Thus, if the substrate temperature is low, the adsorbed atoms present a low mobility within the substrate surface and result in the formation of many small grains with different orientations. If the atom energy is increased by substrate heating, for example, atom diffusion is enhanced and films crystallize forming larger grain sizes. [1]

In our case, for TiN deposition, Ti targets are sputtered in a chamber where the plasma is generated by an Ar/N2 gas mixture. The nitrogen is dissociated within the plasma and results in free radicals that react with Titanium and deposit TiN films. Clearly, the addition of nitrogen species to the plasma can

significantly modify the discharge parameters and strongly influence in the grain formation mechanisms.

In the following sections we will describe the impact of each plasma parameter on the deposited film morphology for an RF-PVD deposition process.

- **Direct Current Voltage**

By modifying the DC voltage, the ion energy can be influenced and the target sputtering yield is controlled. By this, for example, the film deposition rates can be controlled. Besides, the energy flux carried to the substrate by the reflected neutrals is also modified. At high DC powers, the incident ions are very energetic. Their energy is then transferred to the target atoms which are ejected towards the substrate with high kinetic energies. The relaxation of the atom energy at the substrate surface results in the formation of film internal stress that can modify the film structure and morphology. The internal stress relaxation typically results in the formation of large grains. [1]

- **RF Source power**

The RF source power is the responsible of the plasma ignition. When working at higher RF powers, the electronic density is increased, which results in a higher gas dissociation. This results in a larger flux of ions impinging the target and a more important transport of energetic atoms towards the film surface. This will increase the amount of nucleation sites but also the diffusion within the film surface, leading to larger grain sizes [3]. Concerning the RF-PVD TiN deposition process, in our case, the RF source power is superposed to the Direct Current because it permits to decrease the target voltage. This results in a decrease of high energetic species (bombarding the substrate) and therefore a decrease on the High-k damage.

- **Pressure**

The impact of the working pressures on the deposited film morphology is well known in the literature [5] [4] [6]. At high working pressures, the mean free path for the atom diffusion within the plasma is reduced. This leads to an increase of the atom collisions within the plasma before reaching the substrate surface. During these collisions, an overall loss of the atom kinetic energy occurs. Thus, the sputtered particles arrive at the film surface with few or no energy to diffuse which promotes the formation of nucleation sites and small crystal grains. In the case of TiN deposition, other effect should also be considered due to the presence of the N_2 reactive gas. In fact, at equal gas flow, an increase in the working pressure leads to an increase of the particle residence time which promotes plasma-surface reactions.

- **Substrate Bias**

A last parameter that can influence the film morphology is the addition of a superposed substrate bias voltage that attracts ions towards the substrate surface. This bias addition can improve the deposited film morphology by sputtering of unwanted growth boundaries and defaults and forming planar surfaces. Besides, it may give some energy to atoms to diffuse and promotes crystal formation. However, strong ion bombardment also results in the formation of internal stresses that can be detrimental for the film morphology [7] [1]. In our case, it is not possible to use back biasing. However, this is suitable for our processes since, as the TiN is deposited over HfO_2 HK films, working with no applied bias prevents damaging the underlying films.

In conclusion, to modify the morphology of the deposited film we will most likely modify plasma conditions by changing the RF power and working Pressure. In fact, the RF power impacts the plasma electron density (n_e), while the pressure impacts the electron temperature (T_e) and therefore. By playing with these two variables we can control the plasma dissociation and atom energy and therefore, the transfer of metal atoms towards the substrate surface.

Of course, the temperature also has an important role on the deposition conditions since it will influence the atom diffusion. Working at high temperatures allows atom bulk diffusion and uniform crystal formation. Film annealing is also interesting technique to improve the crystallization of the deposited films. In fact, the internal stresses are relaxed and the structure defaults are removed upon heating leading improving the film crystallization and the formation of large grains. Besides, the diffusion and solubility of species (N, O…) increases with temperature and results in the formation of densified films [8] [9]
The relationship between the process conditions and the deposited film morphology were described by Thornton et al. He proposed a diagram as a function of the working pressure and temperature that describes the film morphology evolution with working conditions (Figure X).

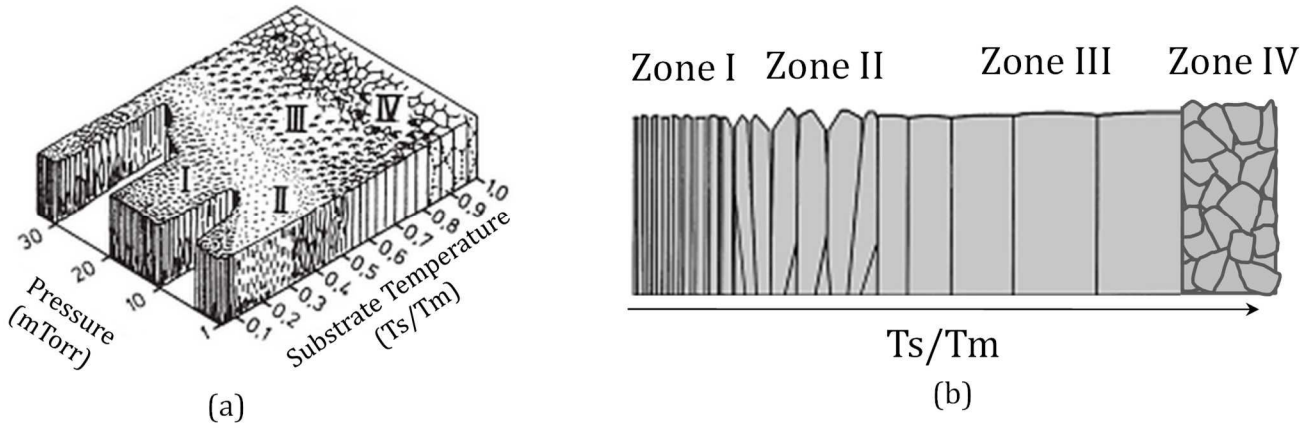

Figure 2. Morphology of PVD deposited films as a function of the working pressure and substrate temperature [1] and a cross section illustration reprinted from *Petrov et al* [2]

Where *T* is the substrate temperature, *Tm* coating material melting point

This diagram is divided in four zones. In Zone 1 (T/Tm<0.3) the grain structure is columnar, and consist in crystal grains defined by voided boundaries. In Zone 3 (0.3<T/Tm<0.5) the columnar grains are wider and are separated by well defined grain boundaries. Zone 2 consists in a transition zone between Zone 1 and Zone 3 where poorly defined fibrous grains are observed. Finally, in Zone 3 (T/Tm>0.5) the high working temperatures allows bulk diffusion and the formation of equiaxed grains.

In the standard deposition conditions, the TiN films are deposited at low pressures (3mT) and low working temperatures (20ºC) and therefore, the TiN film morphology should be similar to that of zone 1. However, it should be considered that very thin TiN films are deposited (3.5-10nm) that present a semi-crystalline-like structure where the TiN grains are distributed within an amorphous TiN phase [5]. Only for higher film thicknesses (50nm or higher) the TiN film is known to crystallize in a columnar fashion [1].
In conclusion, a good control of the deposition conditions is of relevant importance because they can modify the film microstructure including its crystalline grain orientation or film surface roughness, which strongly influences the physical properties of the deposited materials.

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Annex II.

Optimization of SiARC etch chemistries

1. *Optimization of the SiARC etch conditions in CF_4/CH_2F_2*

Since tuning the ion energy to control photoresist sputtering is not enough to limit pattern degradation, the remaining plasma parameters (RF, Pressure, Ratio…) need to be optimized to change the deposition/etch mechanisms and ensure suitable selectivity and satisfying SiARC etch rates.

Figure IV.1 shows SEM cross-section images of Photoresist patterns exposed to different SiARC etch processes. For a better understanding of the etch/deposition mechanisms occurring for each process, top view CD and roughness measurements carried out by CD-SEM are also shown. Due to privacy towards the STMicroelectronics process, the process parameters cannot be detailed.

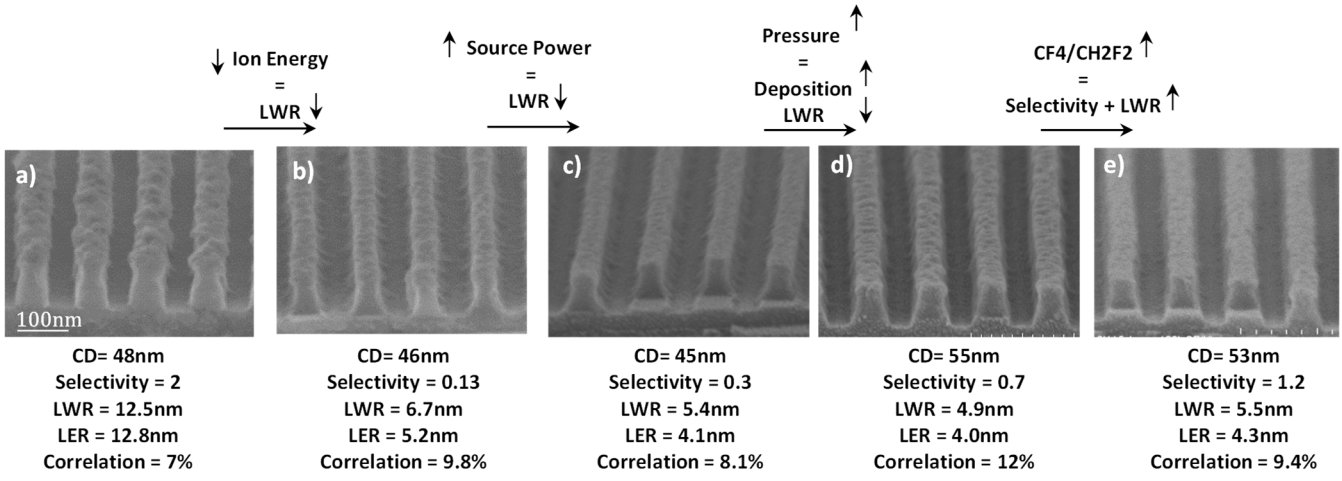


Figure 1 Pattern CD, roughness and correlation evolution with process conditions

The influence of each plasma parameter in the SiARC etch process is described as follows:

Ion energy (Fig 1a&b): Decreasing the ion energy limits resist sputtering and degradation but with a strong increase of polymer deposition. The photoresist presents a strong footing and the SiARC etch process is stopped.

Source Power (Fig 1b&c): Moving to higher source powers increases the gas dissociation. This leads to a higher amount of reactive species available for polymer etching. The FC film deposition is reduced and

the PR etch rate is increased up to 2.1nm/s while the SiARC etch rate remains low (0.7nm/s). This results smoother resist profiles but a poor PR/SiARC selectivity.

Pressure (Fig 1c&d): Most likely, at high source power and low bias (Fig 17c), there is not enough polymer deposition to limit PR erosion or to enhance the SiARC etching by formation of CO and CO_2 volatile compounds. Therefore, to improve PR/SIARC selectivity, working at higher pressures was tested. At high pressures, the radical flux is increased. This leads to an increased deposition of CF_x fluorocarbon species that enhance the SiARC etch rate but limit the photoresist etching. Due to the uniform deposition of FC radicals over the photoresist, the roughness may be slightly improved while the PR/SiARC selectivity is increased. However, the increased deposition leads to a CD widening of 10nm and an increase of the correlation factor up to 12%

CF_4:CH_2F_2 Ratio (Fig 1d&e): A controlled deposition can be obtained by tunning the CF_4:CH_2F_2 ratio while the overall gas mass flow remains constant. Thus, the CF_4/CH_2F_2 ratio was increased from 2:1 to 3:1 to increase the amount of available fluorine for photoresist and fluorocarbon polymer etching. This condition leads to a fluorine rich F/C polymer deposition that increases the final CD of 5nm as compared to the initial condition in Fig 1a. However, the fluorine rich composition of the FC film contributes to SiARC and PR etching improving the selectivity and the sidewall roughness compared to the initial process.

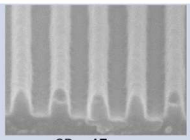
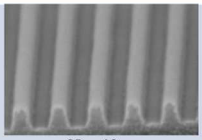
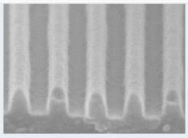
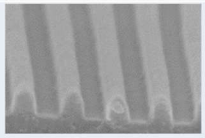
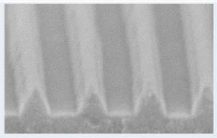
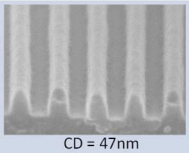
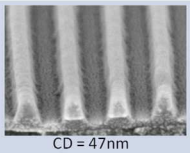
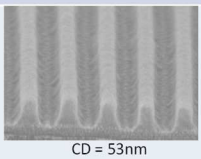
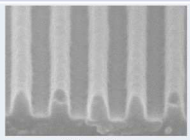
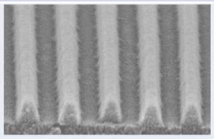
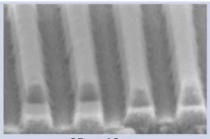
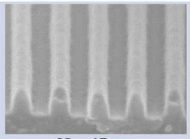
However, despite the many efforts done to optimize the SiARC etch process in CF_4/CH_2F_2, none of the proposed processes seem to be a good candidate for SiARC patterning. Any process in CF_4/CH_2F_2 presents high correlation and roughness values that do not satisfy our patterning requirements. Other plasma chemistries need to be found.

2. Optimization of the SiARC etch conditions in SF_6/CH_2F_2

The influence of each plasma parameter such as Source power, applied DC bias, pressure and gas ratio was also studied for SF_6/CH_2F_2 conditions.

A summary of all the process conditions tested is shown in Table 5. It should be considered that, for all conditions, only one plasma parameter is modified keeping the remaining process conditions constant.

Table 1 Impact of the process condition parameters on the SiARC patterning in SF_6/CH_2F_2

	Low	Middle	High	Conclusions
Source Power		 CD = 47nm LWR = 4,8nm LER = 3,5nm Correlation = 4% Selectivity : 0,9	 CD = 49nm LWR = 5,8nm LER = 4,7nm Correlation = 9% Selectivity : 0,72	- Higher plasma dissociation at high source power - Increased PR etch rate → Selectivity loss - CD and LWR increase
Bias Voltage	 CD = 47nm LWR = 4,8nm LER = 3,5nm Correlation = 4% Selectivity : 0,9	 CD = 49nm LWR = 4,5nm LER = 3,2nm Correlation = 0,3% Selectivity : 0,77	 CD = 45nm LWR = 4,3nm LER = 3,0nm Correlation = 0,1% Selectivity : 0,75	- Higher bias voltage increases ion energy and sputtering. Polymerization is reduced - Increased sputtering increases SiARC etch rate - Low polymerization → PR ER increased →Selectivity loss - Increased PR sputtering leads to tapered profiles and larger CDs. - At higher bias, PR limited budget → SiARC CD loss
Pressure	 CD = 47nm LWR = 4,8nm LER = 3,5nm Correlation = 4% Selectivity : 0,9		 CD = 47nm LWR = 6,4nm LER = 4,5nm Correlation = 0,7% Selectivity : 0,6	- High pressure increases the radical flux - PR etch rate is increased --> Selectivity loss
SF_6/CH_2F_2 ratio	 CD = 53nm LWR = 5,5nm LER = 3,8nm Correlation = 0,3% Selectivity : 0,6	 CD = 47nm LWR = 4,8nm LER = 3,5nm Correlation = 4% Selectivity : 0,9	 CD = 45nm LWR = 5,8nm LER = 4,1nm Correlation = 1,2% Selectivity : 0,7	CH_2F_2 concentration increase - increased CFx species - SiARC etch rate increase → Improved Selectivity If too much CH_2F_2 is added - Strong polymerization - SiARC etch rate decrease → Selectivity loss - Larger CDs and tapered profiles - LWR increased due to tapered profile
N_2 flow (%)	 CD = 49nm LWR = 6,0nm LER = 4,3nm Correlation = 1,2% Selectivity : 0,88	 CD = 47nm LWR = 4,8nm LER = 3,5nm Correlation = 4% Selectivity : 0,9		N_2 enhances plasma dissociation - Enhances the radical formation - Increased Etch rates → Increased Selectivity - Higher radical composition smoothers PR roughness Too high [N_2] dilutes plasma gas phase - Decease of the available reactive species - Decrease SIARC etch rate → Selectivity is improved

The influence of SF_6/CH_2F_2 plasma parameters on the SiARC etch process are described as follows:

Source Power: Increasing source power increases plasma electron density and therefore the molecule dissociation reactions. This leads more reactive plasmas with a higher F and CF_x radical formation that will contribute on the increase of the PR and SiARC etch rate. The PR etch rate is more influenced by the radical flux than that of SiARC, therefore, source power increase leads to an overall selectivity loss. The increased PR sidewall erosion leads to SiARC tapered profiles with larger bottom CD values. At high source powers, higher roughness values are measured which are attributed to a compromised edge detection by CD-SEM due to pattern faceting.

Applied bias: The bias power mainly controls the plasma ion energy. At higher bias voltages, the ion energy is increased and results in an increased PR sputtering and SiARC etch rates. The PR erosion by

energetic ions leads to SiARC tapered profiles and an increase of the pattern bottom CD values. At higher ion energies, the is not enough PR budget to cover the SiARC layer and the SiARC footing is chop-off reducing the final CD. The pattern roughness is seen to decrease of 0.5nm by CD-SEM when moving to higher bias voltages. However, detail analysis of this condition by tilted AFM proved that no roughness smoothing occurred at high bias voltages.

Pressure: At higher pressures, the radical flux is increased. As observed in chapter IV, in SF_6/CH_2F_2 conditions, we already have sufficient reactive species to allow SiARC spontaneous etching. Therefore, the increase of the radical flux has a stronger impact on the PR etch rate (which is increased) compared to the SiARC etch rate, leading to a loss in process selectivity.

SF_6:CH_2F_2 ratio: The variation of the SF_6:CH_2F_2 ratio was done keeping a total mass flow and remaining gas composition constant. Thus by varying the ratio between the etchant and polymerizing species, the process condition can be shifted from a deposition to an etch regime. At high CH_2F_2 ratios, the increased polymerization leads to a strong CD increase and the SiARC etch rate is low. Besides, a roughness increase is also observed due to the increased FC film deposition. When CH_2F_2 polymerizing species are reduced, the excess in CF_x species is removed, improving the SiARC etch rate and the PR/SiARC selectivity. At higher SF_6 concentrations, photoresist sidewall erosion occurs leading to smaller CDs and strong roughness increase.

N_2 flow: Addition of N_2 to gas mixtures often results in complicated deposition/etch reactions. N_2 is known to be inert or few reactive towards photoresist but it can contribute to PR etching reactions by formation of C_xN_y or $C_xN_yH_z$ volatile compounds [1]or sidewall passivation by formation of a-C:N or a-C:N:H deposition films [1]. Besides, N_2 is also known to increase plasma electron density and enhance the radical formation [2] [3]. This can be observed when the N_2 flow is increased. The enhanced radical formation increases PR etch rate. Addition of even more N_2 to the gas mixture will probably result in a plasma chemistry dilution and a reduced radical flux.

From these results it can be concluded that the original SF_6/CH_2F_2 process using soft plasma conditions (RF<500w, P<10mT and 70V) with a % 15 addition of N_2 to the gas mixture is an optimized process condition to ensure suitable PR and SiARC etch rates while keeping correct SiARC profiles.

However, for any condition tested in SF_6/CH_2F_2 based plasmas, a strong photoresist etch rate is observed compared to that of SiARC which compromises the PR/SiARC selectivity due to the limited photoresist budget. Other plasma conditions such as bias pulsing are also tested to evaluate their capability to increase PR/SiARC selectivity.

3. Addition of Bias pulsing

As shown in the previous section, no SiARC etch process optimization is possible by modifying the process conditions. The initial condition in SF_6/CH_2F_2 at low pressures and low ion energies already leads to suitable SiARC patterns with low LWR and correlation values. However, due to the increased PR etch rate in SF_6 based plasmas, the PR budget may become a challenge for the application of these processes in real gate integrations, mostly when long trim or over-etch steps are required.
The LAM Ex reactor presents another parameter that can contribute to optimize the process, the possibility of working in a Bias Pulsing (BP) mode. Working in a BP mode allows controlling the energetic ion exposition during the SiARC process. Thus, in the OFF time, no bias voltage is applied and deposition of reactive radicals is enhanced. Then, during the ON time, the reactive layer is sputtered due to ion bombardment.
In this section, we propose to evaluate the BP mode as a technique to increase the PR budget and PR/SiARC selectivity. For this, long trim times (72s) and SiARC over-etch (50%) where chosen in order

to obtain 20nm final gate CD values. Thus, previously trimmed PR and SiARC samples were etched in SF_6/CH_2F_2 plasmas in a BP mode (200Hz, DC25%) and a CW mode.

Figure 2 shows SEM cross-section images of photoresist and SiARC patterns after exposure to SF_6/CH_2F_2 plasma in a CW mode and compared to a BP mode.

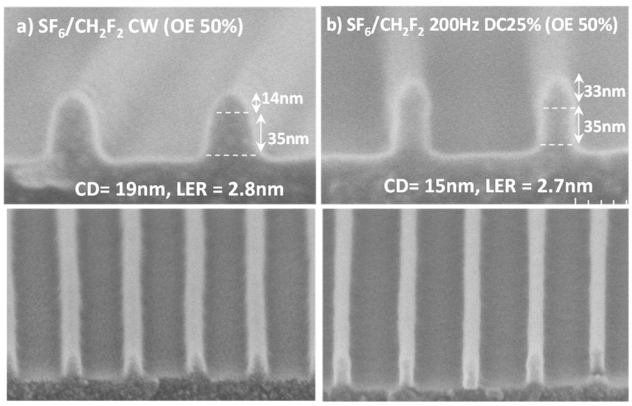


Figure 2 SEM Cross section images of PR and SiARC patterns after exposure to the SiARC etch process in SF_6/CH_2F_2 in a CW (a&b) and BP at 200Hz and DC25% (c&d). CD, Roughness and correlation values were measured by CD-SEM. Remaining PR thickness was verified by ellipsometry over t-BOX patterns.

The change of the plasma processing mode has no impact on the roughness and correlation values. However, a strong improvement of the PR budget is observed. After full SiARC etch process (EndP + OE), only 14nm PR remain over the SiARC pattern in a CW. In revenge, patterns etched in a BP mode present a remaining PR thickness of 33nm.

Etch rate analyses of the exposed samples were carried out over patterned wafers to confirm the observations done in Figure 2.

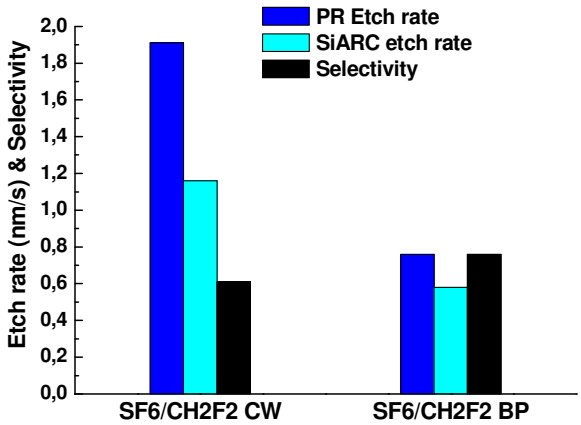


Figure 3 Etch rate and Selectivity of Photoresist and SiARC samples exposed to a SF_6/CH_2F_2 plasma in a CW and BP (200Hz, DC25%)

In a BP condition a SiARC etch rate of 0.6nm/s was calculated, two times lower than the SiARC etch rate in a CW (1.2nm/s). It should be noted that, in a BP mode at a DC at 25%, the substrate is bombarded only a quart of the total process time and therefore, we could have expected a further decrease of the SiARC etch rate. However, as already explained in Chapter IV, the SiARC etch rate in SF_6/CH_2F_2 is not

limited by ion energy since there are enough reactive species available to allow spontaneous SiARC etching. Therefore, we assume in a BP mode, during the off time, the SiARC surface is covered of a CFx film that will enhance the SiARC etch yield when bias is applied (ON time) increasing therefore the SiARC etch rate.

In revenge, the PR etch rate is limited by the amount of fluorine diffusion. Therefore, we suppose that the deposition of a thick FC polymer during the off time limits the F diffusion and decreases of the PR etch rate from 1.9nm/s to 0.8nm/s resulting in an improved PR/SiARC selectivity.

XPS analysis of the surface composition of SiARC and PR samples exposed to SF_6/CH_2F_2 plasma for 10s in both CW and BP mode confirm the presence of an increased FC polymer deposition in BP process conditions (Figure 4)

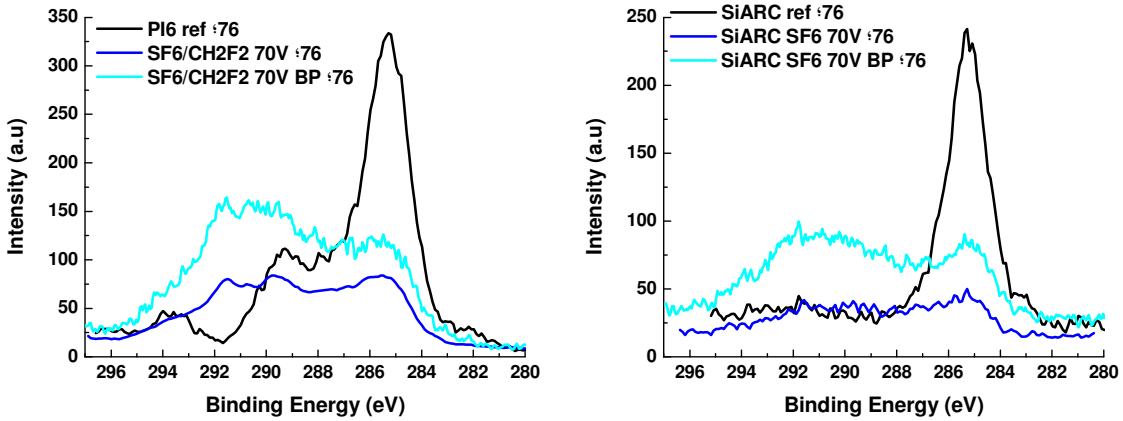


Figure 4 C1s spectra of (a) Photoresist and (b) SiARC samples after exposure to SF_6/CH_2F_2 plasma in a CW and BP. Remaining plasma conditions are the same. Spectra were taken considering the extreme surface composition (θ = 76). The C1s spectra are fitted following the same methodology described in Chapter IV.

In a CW SiARC etch condition, no FC film deposition was observed in SiARC and the PR CF_x contributions observed between 286-293eV were attributed to PR surface fluorination (c.f. Chapter IV). However, in a BP mode, an increased deposition of FC film is observed which is mainly composed of CF_x species at 289.2eV and CF_2 species at 291.3eV.

In conclusion, increased deposition of CFx species in a BP process mode leads to a decrease of the PR and SiARC etch rates but an increase of the PR/SiARC selectivity. These results in an improvement of the PR budget even at extreme process conditions (trim 72s and SiARC OE 50%). Working in a Bias Pulsing mode is therefore a promising technique to improve the SiARC patterning in SF_6/CH_2F_2.

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Annex III

Impact of TiN film thickness on the material properties

To improve the reliability of the AFM technique for the HKMG sidewall roughness metrology, the TiN film thickness has been increased from 3.5nm to 10nm (cf. Chapter V). It is known that TiN microstructure including its crystalline grain orientation or film surface roughness can be different according to the deposited film thickness. In this annex, we compare the surface roughness and microstructure of 3.5nm and 10nm thick TiN films using AFM and XRD techniques in order to determine if important differences exist between the two layers that could compromise the AFM analyses obtained in chapter V.

The main steps for a 14FDSOI HKMG stack preparation are shown in Figure $_2$. High-K Metal Gate stacks are composed of a thin TiN metal film of 3.5nm deposited onto an HfO2 High-K layer of 2nm (Figure 1a). Afterwards a 24nm polysilicon film is deposited (Figure 1b) and annealed at 1000°C for 13s to allow dopants (As, B…) to diffuse within the silicon layer (Fig 1c). Then, the gate stack process continues with the deposition of SiO_2 and Si_3N_4 hard mask stacks and the lithography stacks (PR, SiARC, SoC). The gate patterning process is concluded by subsequent lithography and etch steps. In this deposition process, the TiN layer is thus annealed after the polysilicon deposition.

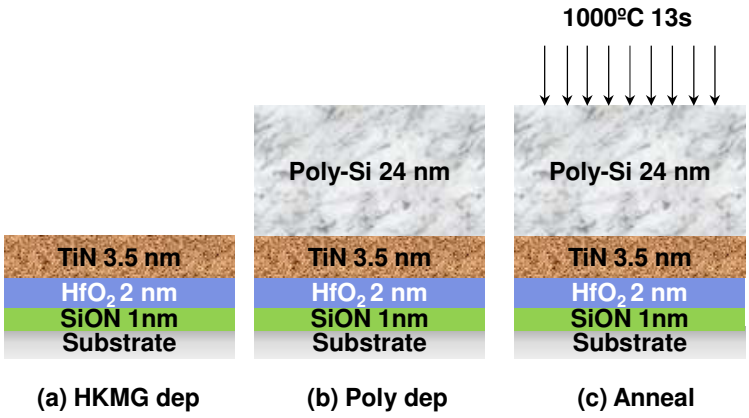

Figure 1 Schematic representation of the HKMG stack after a) HKMG deposition (SiON, HfO2 and TiN), b) polysilicon deposition and c) Source-Drain Anneal.

TiN sample preparation consists of a TiN film deposition at 3mT and 600w at 25ºC with no substrate bias. Such TiN films then follow the HKMG stack process as it is described in Figure 1. After polysilicon deposition and annealing, the Polysilicon/TiN wafers (Figure 1c) are used for the XRD measurements.

However, this configuration does not allow us to measure the TiN film roughness because it is buried under the polysilicon film. Therefore the polysilicon was removed using the wet clean chemistry in HF/NH_4OH proposed in Chapter V.
By this method, the TiN film surface roughness can be measured by AFM over 3.5nm and 10nm TiN films as deposited (at 3mT, 600w and 25ºC (Fig 2 (a&c)), and after full process, which includes polysilicon deposition, annealing at 1000ºC during 13s and polysilicon removal in HF/NH_4OH (Fig 2 b&d).

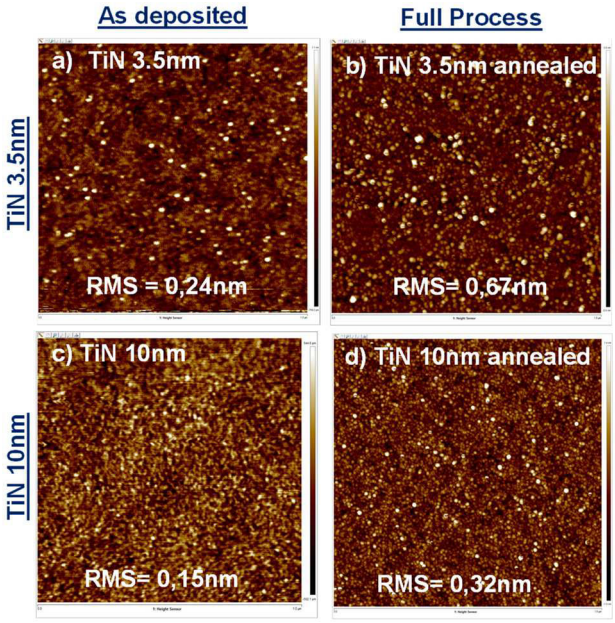

Figure 2 1x1µm AFM images of 3.5nm and 10nm TiN films as deposited at 3mT, 600w and 25ºC (a&c), and after full process: polysilicon deposition, annealing at 1000ºC during 13s and polysilicon removal in HF/NH4OH (b&d).

In a general manner we observe a relatively low surface roughness for TiN films as deposited, whatever the deposited thickness (Fig 2 a&c). This surface roughness is then degraded during the process flow certainly due to the impact of process steps such as polysilicon deposition, annealing or HF/NH4OH wet cleaning. After full process, the 3.5nm and 10nm TiN surface roughness is increased to 0.67nm and 0.32nm respectively (Fig 2 b&d).
Considering that both samples have followed the same sample preparation, the differences on the TiN surface roughness after full process must be related to differences in the TiN surface microstructure.

To better analyze the modifications of the TiN microstructure, XRD analysis of the polysilicon/TiN stacks was carried out.

The X-ray diffraction technique (XRD) allows us to determine the composition, crystallization degree and crystal orientation of a deposited layer. The principle is based in the fact that crystal grains diffract incidence X-ray light. This scattered light is collected and represented as a peak diffractogram as a function of the scattering angle. Each peak position depends on the primitive cell dimensions of the crystal structure and is therefore representative of the film composition and crystal orientation. By considering the ratios between the integrals of each TiN contribution the preferred crystal orientation can be identified. Besides, the sharpness of the XRD peak is related to the crystal grain size. Thus, sharp XRD diffractograms indicate the formation of densely and uniformly packed crystalline structures. In revenge, broad and not defined XRD peaks are representative of weakly crystallized or nearly amorphous film structures. Thus, each XRD spectra is unique and representative of a specific material

composition. **In our experimental conditions, the XRD beam is irradiated tangent to the sample which allows measuring the TiN horizontal grain size (i.e. Grain width) and lateral film texture (refer to Chapter II) that are those that could impact the CD variation.**

The XRD spectra of the analyzed samples are shown in Figure 3.

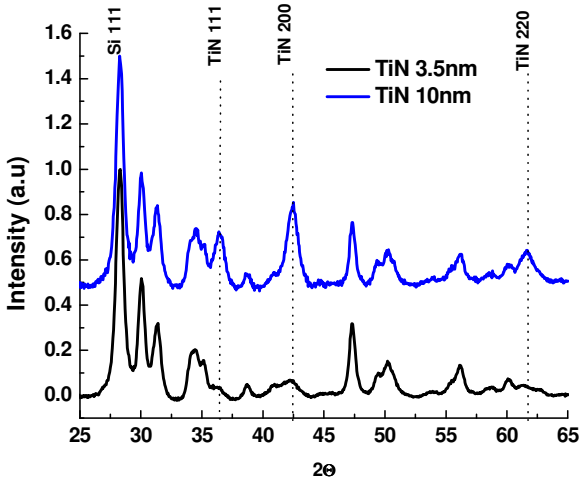

Figure 3 XRD diffractogram of 3.5nm and 10nm TiN films deposed over 10nm HfO2 films and capped with a 24nm polysilicon layer. Spectra are normalized considering the Si [111] peak intensity. For clarity, a 0.5 shift is applied to the 10nm TiN spectra along the Y axis.

For both TiN depositions, the XRD spectra are quite complicated because of the contribution of Polysilicon and crystalline HfO2 peaks. For a better comparison, spectra were normalized by the Si [111] peak intensity at 2θ = 28.24° [1] and only the TIN peak contributions are discussed. For clarity, a 0.5 shift is applied to the 10nm POR spectra along the Y axis.

In the XRD diffractogram of the 10nm TiN film, three TiN crystal structures can be observed which are attributed to the δ-TiN phases with [111] orientation at 2θ=36.46° [2] [3] [4]. [200] orientation at 2θ=42.38° [2] and [220] orientation at 2θ=61.48° [2].

For 3.5nm TiN films, the XRD difractogram presents the same TiN peak contributions, but the 2θ peak positions are slightly shifted towards lower angles (~2θ-0.2). This decrease of the Bragg diffraction angle corresponds to a widening of the crystal lattice which can be attributed to an increase of oxygen diffusion for thin TiN films. This oxygen may come from equipment contamination during the TiN film deposition [5], from TiN surface oxidation in atmosphere during transport [6] or from the underlying HfO_2 film that provides oxygen which will diffuse towards the interfaces during the annealing steps [7].

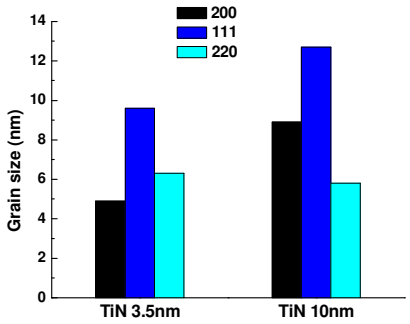

Figure 4 Grain size distribution 3.5nm and 10nm TiN films with δ-TiN phases in [200], [111], and [220] crystal orientation

Concerning the grain size, an overall increase of the horizontal grain size is observed with film thickness. A more important grain size increase is observed for grains in δ-TiN [111] and [200] orientations.

This increase on the grain size dimension with film thickness has already been observed by many authors [2] [8] and is typically attributed to an increased atom mobility due to substrate heating [9] [10] [11], or an increased residual stress formation due to process conditions [12] [13] [14].

However, considering that in our deposition conditions the TiN film is deposited with no applied substrate bias and at low working temperatures (25°C), the increased grain size for 10nm films cannot be attributed to a substrate surface heating or residual stress relaxation but most likely to a phenomenon known as target poisoning [13] [4].

In a TiN PVD deposition a Ti target is bombarded and the sputtered Ti atoms cross a N_2 gas phase where they nitride before reaching the substrate surface. During this process, the Ti target as well as the TiN substrate nitride due to the presence of the N_2 gas phase, which is known as target poisoning. Thus, the TiN film that is deposed by PVD techniques presents a gradient on the nitrogen distribution. The initial TiN layer is a Ti rich TiN that gradually nitrides as the film growths [13]. Therefore, the TiN film deposited at 3.5nm is poorer in nitrogen than the film deposited at 10nm. *Vaz et al* and *Ponon et al* studied the influence of the nitrogen content on the structural properties of TiN thin films [15] [4]. On their studies, they showed that TiN films with stronger nitrogen composition, present wider and denser columns. Therefore, we could imagine that due to the target poisoning effect, TiN films of 10nm are richer in nitrogen and present larger horizontal grain sizes.

From this study, it seems that 3.5 and 10nm thick films do not exactly present the same microstructures and chemical composition. 10nm thick TiN layers have larger horizontal grain size and are richer in nitrogen and poorer in oxygen than 3.5nm thick TiN films. From section V.3.1 of chapter V, it seems that larger horizontal grain size has no impact on the final TiN sidewalls roughness after etching. However it seems that the surface roughness (Figure 2) of TiN film richer in oxygen, as it is the case for 3.5nm thick TiN layer, are more impacted by the final wet cleaning step. Even if not verified, it is suspected that the 3.5nm thick TiN will be rougher after the wet etch than the 10nm thick TiN.

These results are in a good agreement with the observations done in Chapter V and confirm that a different chemical composition in the TiN films may impact the TiN roughness. More particularly, TiN films richer in oxygen present a more important roughness.

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Résumé en Français

L'industrie microélectronique a été l'un des secteurs les plus importants de l'industrie pour ces derniers 60 ans. Le premier transistor a été fait par les laboratoires de Bell à la fin des années 40. Il était composé d'un cristal de germanium pur et sa taille était équivalente à la paume d'une main. Depuis ce jour, l'industrie microélectronique s'est fortement développée. Aujourd'hui, les transistors sont des dispositifs à échelle nanométrique constituées d'un certain nombre de matériaux différents empilés dans des intégrations très complexes. Maintenant, les transistors sont au cœur de la plupart de nos appareils électroniques; des voitures et des téléphones mobiles aux stimulateurs cardiaques, et leurs applications sont innombrables : Automobile, Biologie, Sécurité, Médecine…

Une telle évolution est le résultat des énormes efforts effectués par des ingénieurs et des scientifiques dont le but était d'améliorer le processus de fabrication des transistors afin d'atteindre les meilleures performances. Cela a conduit à une diminution continue de la dimension du transistor et une augmentation de la densité des transistors par puce. Cependant, la quête pour la miniaturisation résulte en une complexité accrue des circuits intégrés et donc, la fabrication des transistors devient de plus en plus difficile.

Pour aider cette complexité croissante, un consortium d'industriels se réunit chaque année et publie une feuille de route internationale (ITRS, pour « International Technology Roadmap for Semiconductors » en anglais), qui définit les objectifs à obtenir par l'industrie des semi-conducteurs. Ainsi, dans un procédé de fabrication du transistor, la définition de la grille est devenue l'une des étapes les plus difficiles à contrôler. Avec la miniaturisation, les spécifications de l'ITRS pour la fabrication des transistors se sont resserrées jusqu'à l'échelle du nanomètre. Une métrologie et un contrôle des procédés extrême sont nécessaires et la dimension critique de la grille (CD) et la rugosité du bord des lignes (LER, pour « Line edge roughness » en anglais) sont devenus deux des paramètres les plus importants à contrôler. En 2011, l'ITRS a affirmé que la non-uniformité dans la dimension de la grille ne doit pas dépasser 10 % du CD visé (pour les technologies de 14nm) tandis que la rugosité ne devrait pas être supérieure à 12 % de la dimension de la grille. C'est à dire, pour un motif de grille de 20nm, l'ITRS prédit une variation maximale de la taille de grille 20 ± 2 nm avec une rugosité de bord (LER) de 1.7nm.

Actuellement, les meilleures conditions de lithographie permettent la définition des motifs de résine photosensible ayant une rugosité minimale 4-5nm et une non-uniformité du CD de l'ordre de 2 %, ce qui sera ensuite transférée dans les couches sous-jacentes par des procédés de gravure par plasma. Cela signifie que pour atteindre les spécifications définies pour les dernières technologies CMOS, des nouvelles stratégies doivent être mises en place pour contrôler et améliorer cette variabilité.

Jusqu'à présent, les traitements de post-lithographie tels que les traitements par plasma ont été introduits pour augmenter la stabilité de la résine et améliorer la rugosité avant le transfert du motif. Cependant, les traitements de post-lithographie classiques ne sont plus efficaces pour répondre aux spécifications des technologies 14nm, où des structures de grille plus complexes sont développées.

Ainsi, l'objectif principal de ce travail de thèse était d'évaluer l'impact des procédés de gravure à la fois sur le contrôle dimensionnel (CD) et la rugosité d'un motif de grille pour les technologies 14FDSOI. Ce travail a été particulièrement dédié à la compréhension des déformations des motifs de grille au cours des procédés de gravure et de l'évolution de LER tout le long d'un empilement de grille comprenant les couches ultra-minces de métal et diélectrique high-k (HKMG) .

Dans un premier temps, nous nous sommes intéressés à l'étude de l'impact des traitements plasma d'HBr sur des motifs de résine 14FDSOI où des complexes structures de grille en deux dimensions (2D) sont définis. En fait, les traitements HBr ont été établis comme des stratégies pour augmenter la stabilité de la résine et améliorer la rugosité et l'uniformité du CD avant le transfert du motif. Cependant, nous avons mis en évidence que, pour les dernières plateformes de résine photosensible 193nm, l'étape de traitement HBr conduit à un phénomène de fluage des résines. Ce fluage est dépendant de la résine photosensible et quand il est observé sur des motifs de grille en 2D il aboutit à ce qu'on appelle le phénomène de décalage de grille (GS pour « gate shifting » en anglais); à savoir, un mauvais positionnement du motif de grille qui se traduit par un mauvais alignement de la grille par rapport aux contacts et qui conduit à une perte de la performance électrique des transistors. Nous avons montré que l'irradiation dans l'ultraviolet lointain (VUV) émis par le plasma HBr est responsable du fluage des résines. Ainsi, pour limiter le décalage de grille, nous avons proposé des conditions de durcissement optimales avec un rayonnement ultraviolet lointain limité. Cependant, alors qu'une faible dose de VUV est nécessaire au cours des traitements par plasma pour limiter le déplacement des grilles, une dose élevée de VUV est obligatoire pour durcir le motif de résine photosensible et empêcher la dégradation de la rugosité pendant les étapes de gravure suivantes (principalement, la gravure de la couche de SIARC). Un compromis doit être trouvé pour limiter la déformation du motif tout en préservant une rugosité approprié. Comme le décalage des grilles est la question clé pour la technologie 14FDSOI, la stratégie adoptée a consisté à introduire des prétraitements des résines avec une faible dose de VUV, tels que les étapes de « Trim » ou étapes de réduction des coté de résine, afin de limiter le fluage de la résine, et donc le déplacement des grilles. La conséquence est que l'étape de gravure SIARC doit être revisitée pour améliorer le transfert global des motifs de grille.

Ainsi, dans une deuxième partie de ce travail, nous avons décidé d'étudier les stratégies de masquage et plus particulièrement, les mécanismes de dégradation des résines photosensibles dans les chimies de gravure SIARC en plasmas de CF_4. Comme il a été observé, les résines sont dégradées dû à la synergie entre la formation d'une couche réactive de fluorocarbone (FC) riche en Carbone et le fort bombardement ionique. Afin de limiter la dégradation de la résine photosensible, nous avons proposé un procédé de gravure différent dans des chimies de SF_6/CH_2F_2 qui empêche le dépôt des FC et permet de travailler à des énergies ioniques plus faibles. Ces conditions permettent d'obtenir des motifs de SIARC appropriés avec une rugosité des flancs de grille contrôlée grâce à l'érosion des aspérités des résines par le fluor ou par l'incidence des ions en angle rasant. Avec ce procédé de gravure de SIARC optimisé (Trim + gravure SIARC en SF_6/CH_2F_2), on obtient des valeurs de décalage des grilles aussi faible que 0,5 nm avec un rugosité des flancs de grille de LER = 2.1 nm, une amélioration considérable par rapport au procédé standard (Cure + gravure de SIARC en CF_4/CH_2F_2), où les valeurs de décalage de grille obtenus sont de environ 6 nm avec des rugosités de bord de grille de environ 2,5 nm. Nous avons ensuite étudié le transfert de la rugosité lors de la structuration des couches de masque dur et

du silicium poly-cristallin. Nous avons montré que les valeurs de décalage des grilles maintenus assez faibles pendant le transfert, mais la rugosité de bord de ligne est légèrement dégradé (LER = 3.3nm mesurée sur le silicium). Nous pensons que c'est l'étape d'ouverture de masque dur la responsable de cette augmentation de rugosité.

Enfin, la dernière partie de ce travail a été consacrée à l'étude de la rugosité lors de la structuration des couches de métal/high-k composant la grille 14FDSOI. Plus particulièrement, l'étude a porté sur l'impact des étapes de gravure HKMG sur la rugosité finale de la grille en métal (TiN). Pour cela, nous avons utilisé une nouvelle technique de métrologie élaborée dans notre laboratoire, la technique d'AFM Tilté. Cette technique nous permet de sonder avec une sonde AFM, les flancs d'un empilement de grille complète, y compris la couche de TiN enterrée. En outre, nous voulions aussi établir une nouvelle méthodologie pour pouvoir mesurer la rugosité du bord de TiN par des techniques de CD-SEM standard. Cette stratégie consiste à éliminer les masques durs et les couches de silicium poly-cristallin en utilisant des solutions chimiques et en laissant le motif de TiN intacte. Les solutions humides dissolvent sans doute les couches passivation déposées sur les flancs de TiN et donc cette technique est représentative de la rugosité de bord des motifs HKMG après le procédé de structuration complet, y compris les étapes de nettoyage humide. En comparant les deux techniques (AFM et CD-SEM), nous pouvons déterminer l'impact des procédés de gravure sèche et humide sur la rugosité de bord des motifs de TiN.

De cette étude, nous concluons que la rugosité de TiN n'est pas largement modifiée au cours du traitement de plasma; cependant, elle est fortement modifiée pendant le procédé de nettoyage par voie humide. Cette modification résulte de la dissolution des couches de passivation de TiN qui sont formés au cours de la gravure. En fonction de la chimie humide choisie, l'impact sur la rugosité du TiN peut varier. Ceci suggère que le traitement par voie humide a un rôle important sur les mécanismes de lissage du TiN. D'ailleurs, nous sommes également intéressés à l'impact de la granulométrie de TiN sur la rugosité du bord de l'empilement HKMG. Selon nos résultats, la taille des grains de TiN n'a pas ou peu d'impact sur la rugosité du TiN. En revanche, la composition chimique du TiN, et plus particulièrement, le contenu en oxygène, a un impact sur la rugosité du TiN. Nos résultats suggèrent que les films de TiN oxydés sont plus sensibles aux solutions humides (i.e. à base d'HF) et sont alors plus dégradés au cours des étapes finales de nettoyage humide. Enfin, il convient remarquer que nos expériences ont été réalisées sur des films de TiN de 10nm qui peuvent différer des films de TiN 3,5 nm utilisés dans de véritables intégrations de grilles. Même si pas vérifié, nous soupçonnons que le TiN d'une épaisseur de 3,5 nm sera plus dégradé après le procédé de nettoyage humide que le TiN de 10nm d'épaisseur.

Au cours de ce travail de thèse, nous avons vu les principaux défis pour l'amélioration du contrôle dimensionnelle dans des motifs de grille 14FDSOI. Nous avons mis au point un nouveau procédé de gravure de grille (avec un trim de résine, une ouverture du SIARC en SF_6/CH_2F_2 et un procédé optimisé de gravure de masque dur) qui permet la définition des motifs de grille de 14nm sans déformations de motif et avec des valeurs de rugosité appropriées. Le déplacement des grilles (i.e. gate shifting) a été réduit de 6 nm jusqu'à 0,5 nm et la rugosité du bord de poly-silicium a été améliorée de 3.3nm à 2.7nm. Les spécifications indiquent que, pour les intégrations 14FDSOI, les motifs de grille doivent être définis avec un décalage des grilles non supérieure à 1 nm et une rugosité du bord maximale de 1.7nm. Selon nos résultats, le procédé développé est approprié, même pour les

très petits motifs de grille, mais il reste loin des spécifications de rugosité définies par l'ITRS (LER = 1.7nm). Ceci révèle qu'il pourrait être également adapté pour la gravure de motifs de grille pour des technologies avancées sub-14nm. Le nouveau procédé proposé a été mis en œuvre à STMicroelectronics et est actuellement testé sur un certain nombre de produits différents. En outre, nous avons montré que les interactions entre les différentes étapes de mise en forme, y compris, lithographie, gravure et nettoyage humide deviennent très importantes et peuvent même être limitants en termes de CD et de contrôle de rugosité de bord. Des efforts conjoints doivent être effectués afin de développer des procédés de gravure de grille qui satisfont aux spécifications de control dimensionnelle.

Pour un travail futur, il serait intéressant d'étudier davantage le phénomène de fluage des résines photosensibles pour des différentes plateformes des résines. Une compréhension plus détaillée des modifications physico-chimiques des polymères au cours du traitement de plasma est nécessaire afin de développer des plateformes de résines plus adaptées. En outre, nous avons souligné l'augmentation de la rugosité du bord au cours du procédé de gravure de masque dur en CF_4/CH_2F_2. L'étude de cette approche est également important pour trouver de nouvelles méthodes pour améliorer la rugosité des bords de grilles tout au long du procédé de gravure. Enfin, nous avons également mis en évidence la forte incidence des conditions de dépôt de TiN et les étapes ultérieures de nettoyage humide sur la modification de la rugosité du TiN. Pour mieux comprendre ces modifications de la rugosité, il serait nécessaire d'effectuer une analyse plus détaillée de la composition de TiN en fonction des conditions de dépôt et d'étudier l'impact de la composition de TiN sur les mécanismes de gravure sèche et humide. Finalement, une comparaison des résultats obtenus sur des couches de TiN déposées par la technique de RF-PVD avec des films de TiN déposés en utilisant d'autres techniques de dépôt, tels que le PE-ALD, serait intéressant pour déterminer si les différentes conditions de dépôt de métal peuvent influer sur la rugosité finale de la grille.

Cette thèse a été effectué dans le cadre d'une collaboration CIFRE entre l'entreprise STMicroeletronics (ST) et le Laboratoire LTM (CNRS). Toutes les expériences ont été réalisées dans un environnement industriel (à savoir, avec un réacteur industriel) et sur de vrais substrats fournis par ST afin de mieux répondre aux défis de l'entreprise en termes de contrôle dimensionnelle et rugosité pour les technologies 14FDSOI. Au début de cette thèse, ce produit était en cours de développement et été prévu pour être délivré en 2015.